FEATURES

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  - Serial Wire Debug Port
  - Deterministic, High-Performance Interrupt Handler
  - Nested Vectored Interrupt Controller (NVIC)
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  - Power on Reset (POR)
  - Reduced Power Modes: Sleep, Deep-Sleep, and Deep Power-Down.
  - External Wakeup through General Purpose Input/Outputs (GPIO) and Dedicated WAKEUP Pin

GENERAL DESCRIPTION

The RC10001 thirty-two bit microcontroller is a full featured processor core and peripherals. It is designed in a high-temperature SOI process to operate from -55ºC to 300ºC reliably. The part operates up to 4MHz.

The ARM Cortex-M0 is the core processor. The ARM core contains a system tick timer, a watchdog timer, a nested vector interrupt controller (NVIC), register banks, and memory. Power control and sleep modes reduce the power consumption. The Cortex-M0 uses the advanced Thumb-2 instruction set.

Peripheral functions include a UART interface, a SPI interface, a LIN interface, four timer/counters with one capture input and four match outputs, a real-time counter, and up to ninety general purpose input/output (GPIO) pins.

The RelChip™ RC10001 32-bit ARM Cortex-M0 microcontroller is designed for extreme environment applications such as down-hole oil, gas, and geothermal applications, automotive, aerospace, industrial control, and utilities.

ARM Cortex-M0 Core

The items unique to the RC10001 implementation of the core are described here. The ARM core is a thirty-two bit machine with sixteen bit Thumb-2 instruction. All control registers and periphery are memory-mapped. This efficient, yet simple core achieves a performance of 0.45DMIPS/MHz on the Dhrystone benchmark.[1] A complete description of the ARM Cortex-M0 can be found in the *ARMv6-M Architecture Reference Manual* and the *Cortex-M0 Technical Reference Manual*.

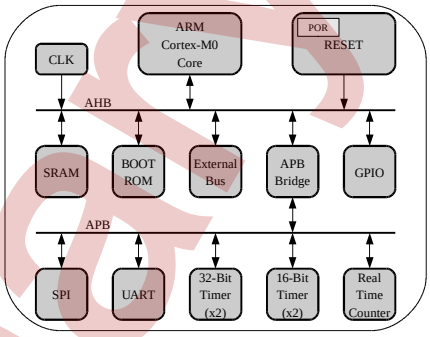

Figure 1: Block Diagram

The RC10001 configuration of the core includes single cycle thirty-two bit multiply, thread and handler modes of processor execution (including two stacks), twenty-six interrupts (six system plus twenty with programmable priority), three sleep modes, serial wire debug, and uses both AHB and APB ARM Buses internally.

Registers

The core contains a register bank, and some special purpose registers. The register bank consists of sixteen thirty-two bit registers. The first eight registers of the bank (R0-R7) are directly accessible by all register instructions. The next eight (R8-R15) are accessible by a subset of the instructions. R13 is the stack pointer (SP), R14 is the link register (LR), and R15 is the program counter (PC).

Two stack registers, the main (MSP) and the process (PSP), are provided to separate the handler and thread mode stacks. Splitting stacks is enabled by the software. Whichever stack register is the current stack pointer is multiplexed into the stack pointer register (SP).

The special purpose registers control processor mode (handler or thread), interrupt enables and masks, interrupt priorities, sleep mode entry and exit, system tick operation and status, and serial wire debug.

System Tick Timer

The system tick timer is a clocked by the system clock and counts down. When zero is reached, a flag is set. If the interrupt is enabled, one is generated. When the timer completes (counts to zero), it is automatically reloaded and started. The count value is a programmable twenty four bit value.

This register is often used to create “time slices” for different processes.

Nested Vector Interrupt Control (NVIC)

The core directly uses six of the twenty seven interrupts (see Table 1). The remaining twenty-one are generated by peripherals in the RC10001, or from an external source. Each interrupt can be enabled or disabled (except Reset, the non-maskable interrupt [NMI], and HardFault interrupt [illegal instruction or memory access]).

The programmable priority can be programmed from 0 to 3 (0 = highest). If two interrupts of the same priority are simultaneously encountered, the one with the lowest execution number will be executed.

[1] http://www.arm.com/products/processors/cortex-m/cortex-m0.php

Table 1: Interrupts

Interrupt	Priority	Description
1=Reset	-2	Reset
2=NMI	-1	Non-Maskable
3=HardFault	0	Faults
11=SVCall	0	Service Call
14=PendSV	0	Pending Service Call
15=SysTick	0	System Tick
16=Wakeup	Program(1)	Wake Up Pin
17=RAM	Program	RAM
18=T16A	Program	Timer/Counter, 16-Bit
19=T16B	Program	Timer/Counter, 16-Bit
20=T32A	Program	Timer/Counter, 32-Bit
21=T32B	Program	Timer/Counter, 32-Bit
22=SSP	Program	SPI Port
23=UART	Program	UART Port
24=WDT	Program	Watchdog Timer
25=SVC1	Program	Service Call
26=GPIO0	Program	General Purpose IO, Port 0
27=GPIO1	Program	General Purpose IO, Port 1
28=GPIO2	Program	General Purpose IO, Port 2
29=GPIO3	Program	General Purpose IO, Port 3
30=GPIO4	Program	General Purpose IO, Port 4
31=GPIO5	Program	General Purpose IO, Port 5
32=GPIO6	Program	General Purpose IO, Port 6
33=GPIO7	Program	General Purpose IO, Port 7
34=RTC	Program	Real Time Clock
35=SVC2	Program	Service Call
36=EXBUS	Program	External Bus

Note 1: Wakeup interrupts can be programmed from multiple sources, including external pins.

Reset Options

Two basic types of reset can occur in the RC10001: a soft reset and a hard reset. A hard reset will first boot the part (i.e. load the code), while a soft reset bypasses the boot load. Both methods then execute an internal reset start.

A hard reset will occur when:

- HARDRESETn is asserted (low).
- Power-on reset (POR) detected for the RAM power supply.
- Power-on reset (POR) detected (with battery backup RAM power), and a boot load has not already occurred.

Soft resets occur when:

- SOFTRESETn is asserted (low).
- A software reset is encountered.
- The watchdog timer expires and the watchdog reset is enabled.
- Power-on reset (POR) detected (with battery backup RAM), and a boot load has already occurred.

Program Boot

The internal memory of the RC10001 is static RAM. The RAM technology is required to reach the high operating temperatures. Four modes to boot the device are provided. These are:

- Boot from the serial wire debug port.
- Boot from the UART port.
- Boot from the SPI port.
- Boot from the external bus.

Clock and Power

The clock is provided by an external crystal and clock oscillator pad pair (see Figure 2). The clock oscillator operates from 1MHz to 4MHz. An external clock generator can drive XTAL1 at frequencies from DC to 4MHz may be used.

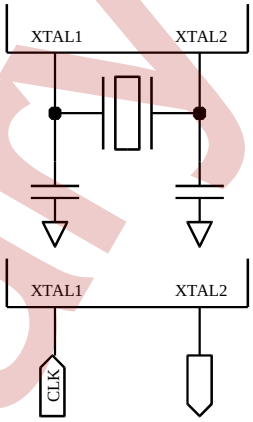

Figure 2: Clock Options

The internal system clock is the external clock divided by an eight-bit value (1 to 255). This internal system clock may or may not be provided to all peripherals (programmable enable). The internal clock may optionally be divided by another eight-bit value for output on the CLKOUT pin.

Sleep Modes

Three sleep modes are used to reduce power. Basic sleep mode disables the clock to the core and memory. Deep sleep mode adds disabling the clock to most peripherals. Deep power-down mode also disables the watchdog timer.

In basic sleep mode, an interrupt generated by any peripheral will “wake up” the microcontroller. In deep sleep mode, thirteen external pins, and the watchdog timer can “wake up” the microcontroller. In deep power-down mode, only the external pins can “wake up” the part.

When individual modules are disabled, the clock to those modules is also disabled, further reducing power required by the controller.

32-Bit Advanced Microcontroller Bus (AHB)

The internal AHB bus is an ARM thirty-two bit, full-frequency, single-cycle bus. The AHB is used for memory (internal and external) and general purpose IO (GPIO) transfers. Also connected to this bus is a bridge to the APB bus. The bus follows the ARM standard.

32-Bit Advanced Peripheral Bus (APB)

The internal APB bus is bridged to the AHB bus. The APB is used for external peripherals. The bus follows the ARM standard.

Memory

The RC10001 contains an internal 4KByte of SRAM for program and data storage. It also contains a boot ROM, not normally accessed by the user. For larger systems, the RC10001 contains a full thirty-two bit, address/data multiplexed external bus. The external bus can address up to 2GByte of external memory.

Memory Map

The RC10001 microcontroller uses memory mapping for peripherals as well as memory. The memory map is shown in Figure 3. About 2GBytes are available for external use. Of this, 1GByte (address 0xA0000000 to 0xE0000000) is available for data storage only.

Memory Parity Checks

Memory parity is checked on a per byte basis. Parity error interrupts for internal SRAM, internal ROM, and external memory may be program enabled.

Internal SRAM

The internal SRAM is 4KBytes. The memory is used for both code and data. Internally, the memory is 32-bits wide with a parity bit per eight bits (total thirty-six bits of width). Parity is calculated during a write of data to the internal SRAM or to external memory. Upon reading the data, parity is checked. A parity error may generate an interrupt (program enabled).

A battery backup circuit for the RAM is available.

Memory Mapped IO

All peripherals are memory mapped. They are mapped as shown in Figure 3. External peripherals are mapped to the device storage area from 3.5GBytes to 4.5GBytes.

ROM Boot Code

The boot code is stored in an internal 1Kbyte ROM. The boot code loads the internal SRAM with the user code from one of four sources selected by the BOOT_SEL[1:0] pins as shown in Table 2.

Table 2: BOOT Selection

BOOT_SEL0	BOOT_SEL1	BOOT Source
0	0	SPI
0	1	UART
1	0	External Bus
1	1	Serial Wire Debug Port

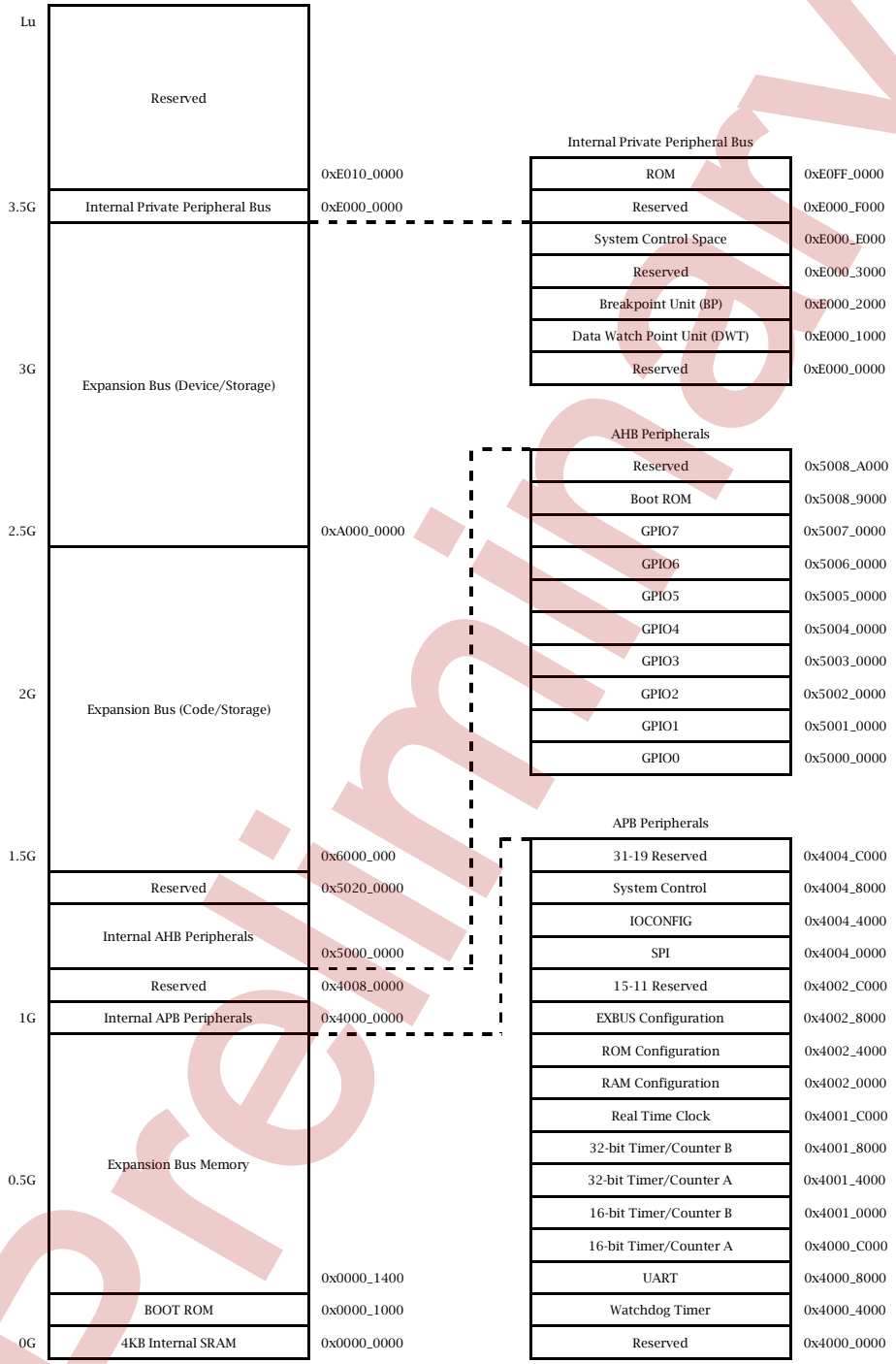

Figure 3: Memory Map

PERIPHERALS

The RC10001 peripherals are designed to maximize applications addressed. The pins serve dual functions: a built in peripheral function (such as UART, SPI, etc.), or GPIO. This is configured on a pin-by-pin basis. Thus, a system can include a SPI, an UART, four timer/counters, and an external bus, or configure some or all of these pins for GPIO.

All GPIO pins are input at reset with either an internal pull-up or pull-down resistor connected. The pull-up, pull-down, input, and output controls are all programmable (see Figure 4).

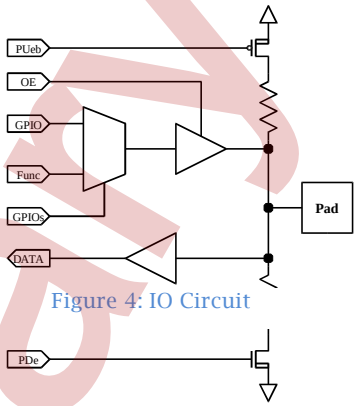

Figure 4: IO Circuit

IO Options

Each of the GPIO pins (90 pins total) can be configured as one of the standard interfaces, or as a GPIO pin. Each of these pins can optionally be configured with pull-up or pull-down resistors. This allows "no connects" in a user application without excessive current flow, or the elimination of external resistors for wire-or connections.

General Purpose IO (GPIO)

Ninety of the pins on the RC10001 can be set for GPIO or configured to a function (see Table 3). Each individual pin (as opposed to the whole port) can be configured as GPIO or as a participant in the function. The input signal is routed to both the function and the GPIO register. The GPIO registers are mask written to avoid spikes on the outputs. This timing is shown in Figure 5.

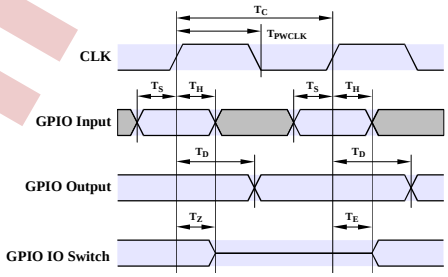

Figure 5: GPIO Waveforms

GPIO pins can be used as input, output, bidirectional, or interrupt input pins. The program switches the pins between these modes. When configured as interrupt inputs, the interrupts can be high level, low level, rising edge, falling edge or both edges.

Table 3: GPIO/Function Pin Selection

Pin	GPIO	Function	Pin	GPIO	Function
SCLK_GPIO0_0	GPIO0[0]	SPI Clock	EBW3n_GPIO4_0	GPIO4[0]	External Bus Byte Write 3
MISO_GPIO0_1	GPIO0[1]	SPI Master Input	EWAIT_GPIO4_1	GPIO4[1]	External Bus Wait
MOSI_GPIO0_2	GPIO0[2]	SPI Master Output	ECRE_GPIO4_2	GPIO4[2]	External Bus Configuration Enable
SSELA_GPIO0_3	GPIO0[3]	SPI Select A	EINT_GPIO4_3	GPIO4[3]	External Bus Interrupt
SSELB_GPIO0_4	GPIO0[4]	SPI Select B	EADQ0_GPIO4_4	GPIO4[4]	External Bus A/D 0
SSELC_GPIO0_5	GPIO0[5]	SPI Select C	EADQ1_GPIO4_5	GPIO4[5]	External Bus A/D 1
SSELD_GPIO0_6	GPIO0[6]	SPI Select D	EADQ2_GPIO4_6	GPIO4[6]	External Bus A/D 2
T16ACAP0_GPIO0_7	GPIO0[7]	Timer 16A Capture	EADQ3_GPIO4_7	GPIO4[7]	External Bus A/D 3
T16AMAT0_GPIO0_8	GPIO0[8]	Timer 16A Match 0	EADQ4_GPIO4_8	GPIO4[8]	External Bus A/D 4
T16AMAT1_GPIO0_9	GPIO0[9]	Timer 16A Match 1	EADQ5_GPIO4_9	GPIO4[9]	External Bus A/D 5
T16AMAT2_GPIO0_10	GPIO0[10]	Timer 16A Match 2	EADQ6_GPIO4_10	GPIO4[10]	External Bus A/D 6
T16AMAT3_GPIO0_11	GPIO0[11]	Timer 16A Match 3	EADQ7_GPIO4_11	GPIO4[11]	External Bus A/D 7
T16BCAP0_GPIO1_0	GPIO1[0]	Timer 16B Capture	EADQ8_GPIO5_0	GPIO5[0]	External Bus A/D 8
T16BMAT0_GPIO1_1	GPIO1[1]	Timer 16B Match 0	EADQ9_GPIO5_1	GPIO5[1]	External Bus A/D 9
T16BMAT1_GPIO1_2	GPIO1[2]	Timer 16B Match 1	EADQ10_GPIO5_2	GPIO5[2]	External Bus A/D 10
T16BMAT2_GPIO1_3	GPIO1[3]	Timer 16B Match 2	EADQ11_GPIO5_3	GPIO5[3]	External Bus A/D 11
T16BMAT3_GPIO1_4	GPIO1[4]	Timer 16B Match 3	EADQ12_GPIO5_4	GPIO5[4]	External Bus A/D 12
T32ACAP0_GPIO1_5	GPIO1[5]	Timer 32A Capture	EADQ13_GPIO5_5	GPIO5[5]	External Bus A/D 13
T32AMAT0_GPIO1_6	GPIO1[6]	Timer 32A Match 0	EADQ14_GPIO5_6	GPIO5[6]	External Bus A/D 14
T32AMAT1_GPIO1_7	GPIO1[7]	Timer 32A Match 1	EADQ15_GPIO5_7	GPIO5[7]	External Bus A/D 15
T32AMAT2_GPIO1_8	GPIO1[8]	Timer 32A Match 2	EADQ16_GPIO5_8	GPIO5[8]	External Bus A/D 16
T32AMAT3_GPIO1_9	GPIO1[9]	Timer 32A Match 3	EADQ17_GPIO5_9	GPIO5[9]	External Bus A/D 17
T32BCAP0_GPIO1_10	GPIO1[10]	Timer 32B Capture	EADQ18_GPIO5_10	GPIO5[10]	External Bus A/D 18
T32BMAT0_GPIO1_11	GPIO1[11]	Timer 32B Match 0	EADQ19_GPIO5_11	GPIO5[11]	External Bus A/D 19
T32BMAT1_GPIO2_0	GPIO2[0]	Timer 32B Match 1	EADQ20_GPIO6_0	GPIO6[0]	External Bus A/D 20
T32BMAT2_GPIO2_1	GPIO2[1]	Timer 32B Match 2	EADQ21_GPIO6_1	GPIO6[1]	External Bus A/D 21
T32BMAT3_GPIO2_2	GPIO2[2]	Timer 32B Match 3	EADQ22_GPIO6_2	GPIO6[2]	External Bus A/D 22
RxD_GPIO2_3	GPIO2[3]	UART Receive Data	EADQ23_GPIO6_3	GPIO6[3]	External Bus A/D 23
TxD_GPIO2_4	GPIO2[4]	UART Transmit Data	EADQ24_GPIO6_4	GPIO6[4]	External Bus A/D 24
CTSn_GPIO2_5	GPIO2[5]	UART Clear-to-Send	EADQ25_GPIO6_5	GPIO6[5]	External Bus A/D 25
DSRn_GPIO2_6	GPIO2[6]	UART Data Ready	EADQ26_GPIO6_6	GPIO6[6]	External Bus A/D 26
RIn_GPIO2_7	GPIO2[7]	UART Ring	EADQ27_GPIO6_7	GPIO6[7]	External Bus A/D 27
DCDn_GPIO2_8	GPIO2[8]	UART Carrier Detect	EADQ28_GPIO6_8	GPIO6[8]	External Bus A/D 28
RTSn_GPIO2_9	GPIO2[9]	UART Request-to-Send	EADQ29_GPIO6_9	GPIO6[9]	External Bus A/D 29
DTRn_GPIO2_10	GPIO2[10]	UART Terminal Ready	EADQ30_GPIO6_10	GPIO6[10]	External Bus A/D 30
OUT1n_GPIO2_11	GPIO2[11]	UART Output 1	EADQ31_GPIO6_11	GPIO6[11]	External Bus A/D 31
OUT2n_GPIO3_0	GPIO3[0]	UART Output 2	EPDQ0_GPIO7_0	GPIO7[0]	External Bus Parity 0
ECLK_GPIO3_1	GPIO3[1]	External Bus Clock	EPDQ1_GPIO7_1	GPIO7[1]	External Bus Parity 1
EACSAn_GPIO3_2	GPIO3[2]	External Bus Chip Select A	EPDQ2_GPIO7_2	GPIO7[2]	External Bus Parity 2
EACSBn_GPIO3_3	GPIO3[3]	External Bus Chip Select B	EPDQ3_GPIO7_3	GPIO7[3]	External Bus Parity 3
EACSCn_GPIO3_4	GPIO3[4]	External Bus Chip Select C	SWCLK_GPIO7_4	GPIO7[4]	Serial Debug Clock
EACSDn_GPIO3_5	GPIO3[5]	External Bus Chip Select D	SWDIO_GPIO7_5	GPIO7[5]	Serial Debug Data
EADVn_GPIO3_6	GPIO3[6]	External Bus Address Strobe			
EWEn_GPIO3_7	GPIO3[7]	External Bus Write Enable			
EOEn_GPIO3_8	GPIO3[8]	External Bus Output Enable			
EBW0n_GPIO3_9	GPIO3[9]	External Bus Byte Write 0			
EBW1n_GPIO3_10	GPIO3[10]	External Bus Byte Write 1			
EBW2n_GPIO3_11	GPIO3[11]	External Bus Byte Write 2			

Universal Asynchronous Receiver/Transmitter (UART)

The UART is a 16550-compatible part. It supports both RS232 and RS485 protocols as well as LIN 2.0. The UART includes:

- Programmable baud rate generator: DC to 1Mbaud
- Protocols
  - RS232
  - RS485
  - LIN 2.0
- First in, first out buffers (FIFO)
  - Separate Transmit and Receive
  - Sixteen byte deep
  - Interrupt triggers at 1, 4, 8, or 14 bytes
  - Maskable
- Communication bits
  - Start
  - 1 or 2 stop bits
  - Even, odd, stick, or no-parity options
- 5, 6, 7, or 8 bit data
- False start bit detection
- Line break generation and detection
- Independent masking
  - Transmit FIFO
  - Receive FIFO
  - Receive Timeout
  - Modem Status
  - Error code conditions
- Modem control functions
  - CTS: Clear to send
  - RTS: Request to send
  - DSR: Data set ready
  - DTR: Data terminal ready
  - DCD: Carrier detect
  - RI: Ring Indicator
  - OUT1, OUT2: Outputs

Local Interconnect Network (LIN)

The UART and one of the thirty-two bit timers are used to implement the LIN 2.0 interface.

When receiving data, the hardware detects a Synch Break followed by a Synch Data field. The Sync Data field is used to auto detect the baud rate. Data is then received through the UART receive FIFO.

When transmitting data, the hardware sends the Sync Break (programmable from 13 to 16 bit times), followed by the UART transmit data FIFO contents.

Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI), also called the Synchronous Serial Port (SSP), is a configurable serial interface. This serial interface can be configured as a Motorola Serial Peripheral Interface (SPI™), a 4-wire synchronous serial interface (SSI), or a National Semiconductor Microwire™ bus. The part can be configured as the master, or as the slave, serial connection. The port features include:

- Master or slave node
- Full-duplex four wire transmission
- Data rate
  - Programmable from DC 1Mbit per second
  - Programmable clock polarity
  - Programmable clock phase
- Transmit and receive FIFO
  - Eight deep by sixteen bits wide
- Data
  - Programmable size from four to sixteen bits
  - Programmable frame format: SPI, SSI, or Microwire
- Programmable Interrupts
  - Transmit FIFO
  - Receive FIFO
  - Receive FIFO overrun
  - Receive data after idle period
- Loopback test mode

Timer/Counters

The RC10001 contains four timer/counters, two sixteen bit and two thirty-two bit. The timer/counters have internal pre-scalars, four match registers (and outputs), a capture input, a PWM mode, and a NOS (non-overlapping signal) mode. Each timer/counter contains one counter register (CNT), one capture register (CAP), and four match registers (MAT0-MAT3).

Table 4: Timer/Counter Pins

Generic	Timer 16A	Timer 16B	Timer 32A	Timer 32B
Capture	T16ACAP0	T16BCAP0	T32ACAP0	T32BCAP0
Match 0	T16AMAT0	T16BMAT0	T32AMAT0	T32BMAT0
Match 1	T16AMAT1	T16BMAT1	T32AMAT1	T32BMAT1
Match 2	T16AMAT2	T16BMAT2	T32AMAT2	T32BMAT2
Match 3	T16AMAT3	T16BMAT3	T32AMAT3	T32BMAT3

The two sixteen bit counter registers have corresponding sixteen bit pre-scalars while the thirty-two bit counter registers have thirty-two bit pre-scalars. The counter register can be reset by a match register (programmable). Each match register can be programmed to be in normal, PWM, or NOS mode. The capture input can be used as the clock input for the counter register, of the internal clock can be used.

Capture

The capture input is used as trigger input. Events on the capture pins cause the value from the counter register (CNT) to be written into the capture register (CAP). Possible events are a rising edge, a falling edge, or either edge. This write can, if enabled, generate an interrupt. A capture of a rising event is shown in Figure 6. The count value valid is shown in red.

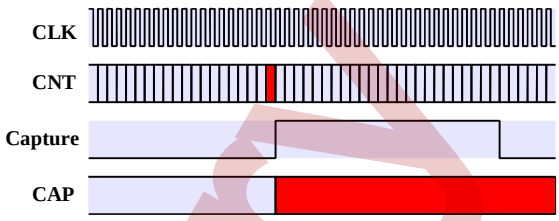

Figure 6: Timer/Counter Capture

Counter

-The capture input can be the clock input to the counter register (CNT). Thus, the capture pin events will be counted. These events can be rising edges, falling edges, or both edges. An example of counting on both edges is shown in Figure 7.

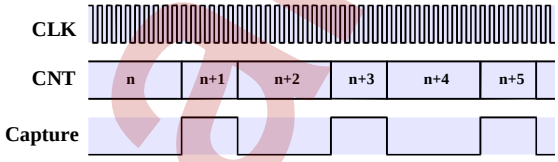

Figure 7: Timer/Counter Counter

Timer Match (normal)

The match registers (MAT0 to MAT3) generate a match event whenever the value of the match register equals the value of the counter register. The event causes one or more actions based upon the configuration programmed. The event can reset the counter, stop the counter, generate a signal on the associated match output pin, and/or generate an interrupt.

Possible events on the match output pins are set high, set low, or toggle. The match output can be inverted in the configuration. The example shown in Figure 8 illustrates this. In the example, match 0 is programmed to reset the counter at count 16. Match 1 is programmed to match at count 2, and invert the match 1 output pin. Match 2 is programmed to match at count 6, and set the match 2 output pin high. Match 3 is programmed to match at count 12, and set the match 3 output pin low.

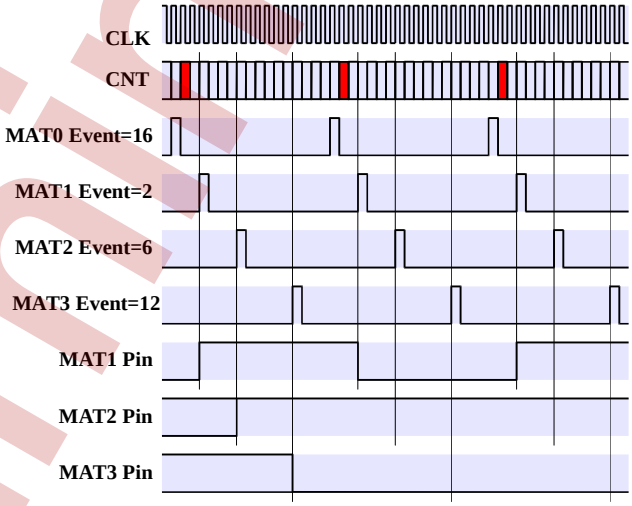

Figure 8: Timer/Counter Match

PWM Mode

In PWM mode, one of the match registers (MAT0-3) is used as a reset for the counter register. This sets the period. The other three are configured to set the match output to a one on a match. When CNT is reset, all match outputs are cleared. The output may or may not

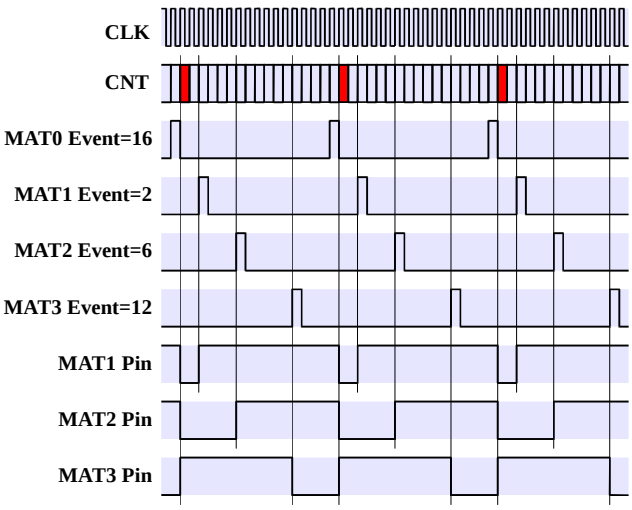

Figure 9: Timer/Counter PWM

be inverted. This mode is useful to generate multiple pulses of varying length where one edge is coincident.

A sample PWM output is shown in Figure 9. In this example, match 0 is used for the period, while the outputs are match 1 through 3. Further, match 3 has been inverted.

Non-Overlapping Signals

A combination of match outputs can be used to set non-overlapping outputs. In this mode, match 0 and 1 events are used to generate the period and one of the pulses, while match 2 and 3 generate the other pulse. Match 0 is fixed for the period. Match 1 is used as the start time for one pulse. This pulse terminates at the end of the period. Match 2 and 3 are used to generate the second pulse. This pulse starts when there is a match 2, and ends when there is a match 3.

The match output pins are used as the non-overlap outputs. MAT0 is the positive pulse generated by match 0 and 1. MAT1 is the inverse of that signal. MAT2 is the positive pulse generated by match 2 and 3. MAT3 is the inverse of that signal. An example is shown in Figure 10.

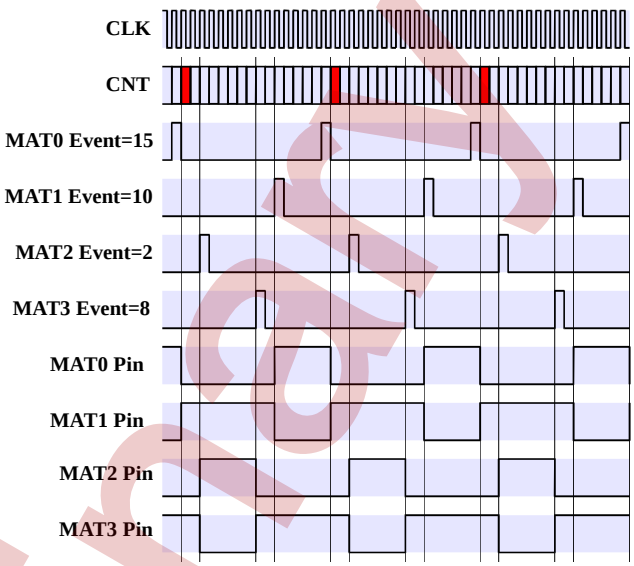

Figure 10: Timer/Counter Non-Overlapping Signals

Local Interconnect Network (LIN) Mode and the Timers

A thirty-two bit timer is used for baud detection and synchronization, while the UART registers and FIFOs are used for the rest of the interface.

Watchdog Timer

The watchdog timer is a twenty-four bit countdown register. When it reaches 0, the microcontroller is reset or an interrupt is generated. It can be disabled.

Real Time Counter

The real time counter can be used as a counter or a clock. The twenty four bit counter increments by one each time the pre-scalar completes (binary mode). In the clock mode, the day, hour, minute, second, and 0.1 second value are output. The pre-scalar is a programmable twenty-four bit divider of the system clock.

External Bus

The external bus is an address/data multiplexed bus. The bus can be configured for eight-bit or thirty-two bit data. The bus uses up to thirty-two bits of address. The bus characteristics are:

- Thirty-two or eight-bit data
- Up to thirty-two bit address
- Four parity bits, one per byte
  - Parity bit, or
  - Parity interrupt flag, or
  - Extra data bit
- Four chip selects
- Byte enabled write (byte masking)
- Output enable for external devices
- Programmable latency, or driven by the WAIT function
- Wired-or bus interrupt for external devices

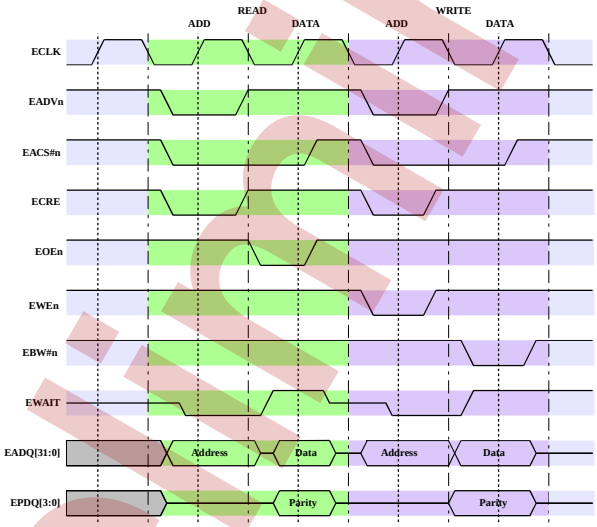

Figure 11: Thirty-two Bit External Bus Transfers

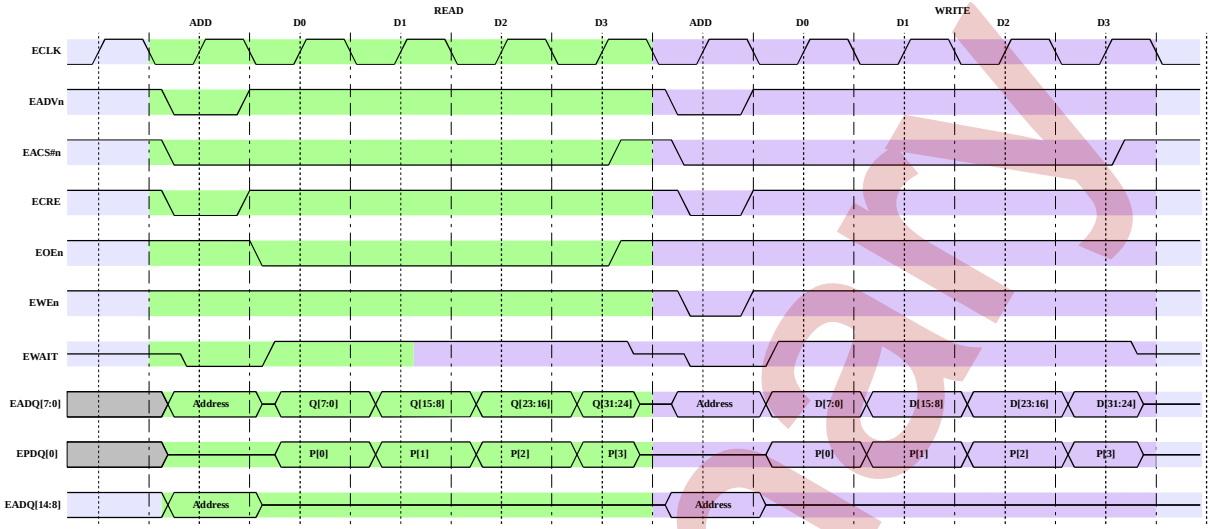

Figure 12: 8-Bit External Bus Transfers

SPECIFICATIONS

Absolute Maximums (1)

Temperature ..... -55 to 350ºC
Power Supply (V_{DD} referenced to ground) ..... -0.3 to 6.0 volts
Battery Voltage (V_{DDB} referenced to ground) ..... -0.3 to 6.0 volts
IO Voltage (referenced to ground) ..... -0.3 to 6.0 volts

Operating Conditions

Temperature (die) ..... -55 to 300ºC
Power Supply (V_{DD} referenced to ground) ..... 4.5 to 5.5 volts
Battery Voltage (V_{DDB} referenced to ground) ..... 3.4 to (V_{DD}-0.1) volts
IO Voltage (referenced to ground) ..... 0.2 to (V_{DD}+0.2) volts

1. Exceeding the maximum specifications may cause permanent damage to the part

DC Characteristics

Table 5: DC Characteristics

Symbol	Description	Min	Typ	Max @225C	Max @300C	Unit	Note
T	Die Temperature	-55	25	225	300	ºC	
V_{DD}	Power Supply	4.5	5	5.5	5.5	V	
V_{DDB}	Battery Power Supply	3.4		V_{DD}-0.1	V_{DD}-0.1	V	1
I_{DDA1}	Active Current (all Clocks Enabled)			TBD	TBD	mA/MHz	2
I_{DDA2}	Active Current (min Clocks Enabled)			TBD	TBD	mA/MHz	2
I_{DDB}	Battery Current (V_{DD}=0)			TBD	TBD	mA	3
V_{OH}	Output High Voltage (I_{OH}=2mA)	0.9*V_{DD}				V	
V_{OL}	Output Low Voltage (I_{OL}=2mA)				0.5	V	
V_{IH}	Input High Voltage	0.8*V_{DD}				V	
V_{IL}	Input Low Voltage				1.0	V	
I_I	Input Current				10	uA	
I_O	Output Current (in Tri-State)				20	uA	

Notes:

1. Battery Backup only available with 5 volt IO voltage.
2. No Output Load.
3. For systems not using battery backup, connect V_{DDB} to GND.

AC Characteristics

Table 6: AC Characteristics

Symbol	Description	Min	Max @225C	Max @300C	Unit	Note
F	Frequency	0	4	3.5	MHz	
T_{PWCLK}	CLK Duty Cycle	45		55	%	

PACKAGING

The RC10001 is packaged as a 144 pin QFP.

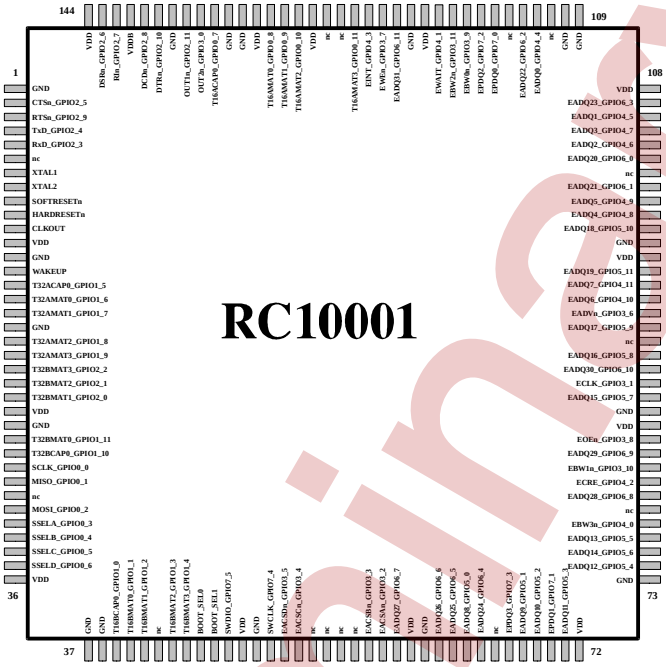

Figure 13: 144-Pin QFP Package

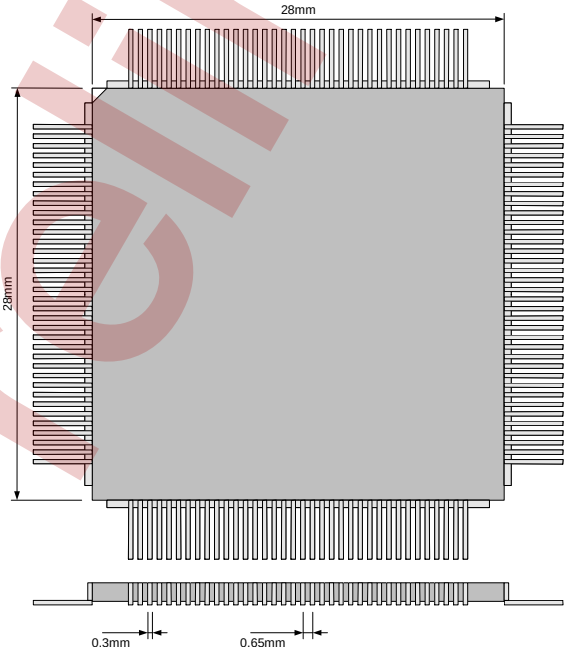

Table 7: Pin Out

Pin	Symbol	Type	Default	Function	Pin	Symbol	Type	Default	Description
1	GND	PWR	na	Ground	73	GND	PWR	na	Ground
2	CTSn_GPIO2_5	I/O	I;PU	UART: Clear to Send	74	EADQ12_GPIO5_4	I/O	I;PU	External Address/Data
3	RTSn_GPIO2_9	I/O	I;PU	UART: Request to Send	75	EADQ14_GPIO5_6	I/O	I;PU	External Address/Data
4	TxD_GPIO2_4	I/O	I;PU	UART: Transmit Data	76	EADQ13_GPIO5_5	I/O	I;PU	External Address/Data
5	RxD_GPIO2_3	I/O	I;PU	UART: Receive Data	77	EBW3n_GPIO4_0	I/O	I;PU	External Byte Write
6	nc	na	na	No Connect	78	nc	na	na	No Connect
7	XTAL1	I	na	Oscillator Input	79	EADQ28_GPIO6_8	I/O	I;PU	External Address/Data
8	XTAL2	O	na	Oscillator Output	80	ECRE_GPIO4_2	I/O	I;PU	External Control Register
9	SOFTRESETn	I	I;PU	Reset	81	EBW1n_GPIO3_10	I/O	I;PU	External Byte Write
10	HARDRESETn	I	I;PU	Reset	82	EADQ29_GPIO6_9	I/O	I;PU	External Address/Data
11	CLKOUT	O	O	Clock Output	83	EOEn_GPIO3_8	I/O	I;PU	External Output Enable
12	VDD	PWR	na	Power	84	VDD	PWR	na	Power
13	GND	PWR	na	Ground	85	GND	PWR	na	Ground
14	WAKEUP	I	I;PU	Wakeup	86	EADQ15_GPIO5_7	I/O	I;PU	External Address/Data
15	T32ACAP0_GPIO1_5	I/O	I;PU	T32 Capture	87	ECLK_GPIO3_1	I/O	I;PU	External Clock
16	T32AMAT0_GPIO1_6	I/O	I;PU	T32 Match	88	EADQ30_GPIO6_10	I/O	I;PU	External Address/Data
17	T32AMAT1_GPIO1_7	I/O	I;PU	T32 Match	89	EADQ16_GPIO5_8	I/O	I;PU	External Address/Data
18	nc	na	na	No Connect	90	nc	na	na	No Connect
19	T32AMAT2_GPIO1_8	I/O	I;PU	T32 Match	91	EADQ17_GPIO5_9	I/O	I;PU	External Address/Data
20	T32AMAT3_GPIO1_9	I/O	I;PU	T32 Match	92	EADVn_GPIO3_6	I/O	I;PU	External Address Valid
21	T32BMAT3_GPIO2_2	I/O	I;PU	T32 Match	93	EADQ6_GPIO4_10	I/O	I;PU	External Address/Data
22	T32BMAT2_GPIO2_1	I/O	I;PU	T32 Match	94	EADQ7_GPIO4_11	I/O	I;PU	External Address/Data
23	T32BMAT1_GPIO2_0	I/O	I;PU	T32 Match	95	EADQ19_GPIO5_11	I/O	I;PU	External Address/Data
24	VDD	PWR	na	Power	96	VDD	PWR	na	Power
25	GND	PWR	na	Ground	97	GND	PWR	na	Ground
26	T32BMAT0_GPIO1_11	I/O	I;PU	T32 Match	98	EADQ18_GPIO5_10	I/O	I;PU	External Address/Data
27	T32BCAP0_GPIO1_10	I/O	I;PU	T32 Match	99	EADQ4_GPIO4_8	I/O	I;PU	External Address/Data
28	SCLK_GPIO0_0	I/O	I;PU	SPI Clock	100	EADQ5_GPIO4_9	I/O	I;PU	External Address/Data
29	MISO_GPIO0_1	I/O	I;PU	SPI Master In	101	EADQ21_GPIO6_1	I/O	I;PU	External Address/Data
30	nc	na	na	No Connect	102	nc	na	na	No Connect
31	MOSI_GPIO0_2	I/O	I;PU	SPI Master Out	103	EADQ20_GPIO6_0	I/O	I;PU	External Address/Data
32	SSELA_GPIO0_3	I/O	I;PU	SPI Select	104	EADQ2_GPIO4_6	I/O	I;PU	External Address/Data
33	SSELB_GPIO0_4	I/O	I;PU	SPI Select	105	EADQ3_GPIO4_7	I/O	I;PU	External Address/Data
34	SSELC_GPIO0_5	I/O	I;PU	SPI Select	106	EADQ1_GPIO4_5	I/O	I;PU	External Address/Data
35	SSELD_GPIO0_6	I/O	I;PU	SPI Select	107	EADQ23_GPIO6_3	I/O	I;PU	External Address/Data
36	VDD	PWR	na	Power	108	VDD	PWR	na	Power
37	GND	PWR	na	Ground	109	GND	PWR	na	Ground
38	GND	PWR	na	Ground	110	GND	PWR	na	Ground
39	T16BCAP0_GPIO1_0	I/O	I;PU	T16 Capture	111	nc	na	na	No Connect
40	T16BMAT0_GPIO1_1	I/O	I;PU	T16 Match	112	EADQ0_GPIO4_4	I/O	I;PU	External Address/Data
41	T16BMAT1_GPIO1_2	I/O	I;PU	T16 Match	113	EADQ22_GPIO6_2	I/O	I;PU	External Address/Data
42	nc	na	na	No Connect	114	nc	na	na	No Connect
43	T16BMAT2_GPIO1_3	I/O	I;PU	T16 Match	115	EPDQ0_GPIO7_0	I/O	I;PU	External Address/Data
44	T16BMAT3_GPIO1_4	I/O	I;PU	T16 Match	116	EPDQ2_GPIO7_2	I/O	I;PU	External Address/Data
45	BOOT_SEL0	I	I;PD	Boot Select	117	EBW0n_GPIO3_9	I/O	I;PU	External Byte Write
46	BOOT_SEL1	I	I;PD	Boot Select	118	EBW2n_GPIO3_11	I/O	I;PU	External Byte Write
47	SWDIO_GPIO7_5	I/O	I;PD	Serial Wire Data	119	EWAIT_GPIO4_1	I/O	I;PU	External Wait for Slave
48	VDD	PWR	Na	Power	120	VDD	PWR	Na	Power
49	GND	PWR	Na	Ground	121	GND	PWR	Na	Ground
50	SWCLK_GPIO7_4	I/O	I;PD	Serial Wire Clock	122	EADQ31_GPIO6_11	I/O	I;PU	External Address/Data
51	EACSDn_GPIO3_5	I/O	I;PU	External Chip Select	123	EWEn_GPIO3_7	I/O	I;PU	External Write
52	EACSCn_GPIO3_4	I/O	I;PU	External Chip Select	124	EINT_GPIO4_3	I/O	I;PU	External Interrupt
53	nc	na	na	No Connect	125	T16AMAT3_GPIO0_11	I/O	I;PU	T16 Match
54	nc	na	na	No Connect	126	nc	na	na	No Connect
55	nc	na	na	No Connect	127	nc	na	na	No Connect
56	nc	na	na	No Connect	128	VDD	PWR	na	Power
57	EACSBn_GPIO3_3	I/O	I;PU	External Chip Select	129	T16AMAT2_GPIO0_10	I/O	I;PU	T16 Match
58	EACSAn_GPIO3_2	I/O	I;PU	External Chip Select	130	T16AMAT1_GPIO0_9	I/O	I;PU	T16 Match
59	EADQ27_GPIO6_7	I/O	I;PU	External Address/Data	131	T16AMAT0_GPIO0_8	I/O	I;PU	T16 Match
60	VDD	PWR	na	Power	132	VDD	PWR	na	Power
61	GND	PWR	na	Ground	133	GND	PWR	na	Ground
62	EADQ26_GPIO6_6	I/O	I;PU	External Address/Data	134	GND	PWR	na	Ground
63	EADQ25_GPIO6_5	I/O	I;PU	External Address/Data	135	T16ACAP0_GPIO0_7	I/O	I;PU	T16 Capture
64	EADQ8_GPIO5_0	I/O	I;PU	External Address/Data	136	OUT2n_GPIO3_0	I/O	I;PU	UART Output
65	EADQ24_GPIO6_4	I/O	I;PU	External Address/Data	137	OUT1n_GPIO2_11	I/O	I;PU	UART Output
66	nc	na	na	No Connect	138	GND	PWR	na	Ground
67	EPDQ3_GPIO7_3	I/O	I;PU	External Address/Data	139	DTRn_GPIO2_10	I/O	I;PU	UART Data Terminal
68	EADQ9_GPIO5_1	I/O	I;PU	External Address/Data	140	DCDn_GPIO2_8	I/O	I;PU	UART Carrier Detect
69	EADQ10_GPIO5_2	I/O	I;PU	External Address/Data	141	VDDB	PWR	na	Battery Power
70	EPDQ1_GPIO7_1	I/O	I;PU	External Address/Data	142	RIn_GPIO2_7	I/O	I;PU	UART Ring
71	EADQ11_GPIO5_3	I/O	I;PU	External Address/Data	143	DSRn_GPIO2_6	I/O	I;PU	UART Data Set
72	VDD	PWR	na	Power	144	VDD	PWR	na	Power

Definitions for the table above:

I – input

O – output

I/O - bi-directional input or output

PU – weak pull-up transistor connected to the output

PD- weak pull-down transistor connected to the output