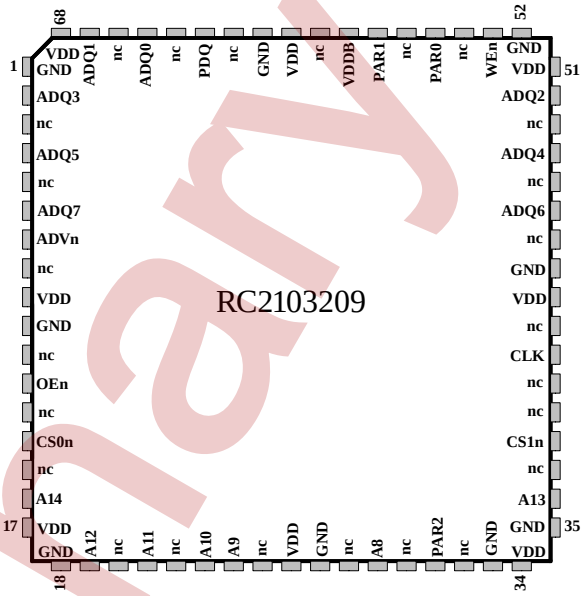
FEATURES

- 32K x 9 Random Access Memory
- 5 volt Operation
- 3.4 volt Battery Back Up
- Fully Static Design
- Wide Operating Temperature Range
- Parity Options



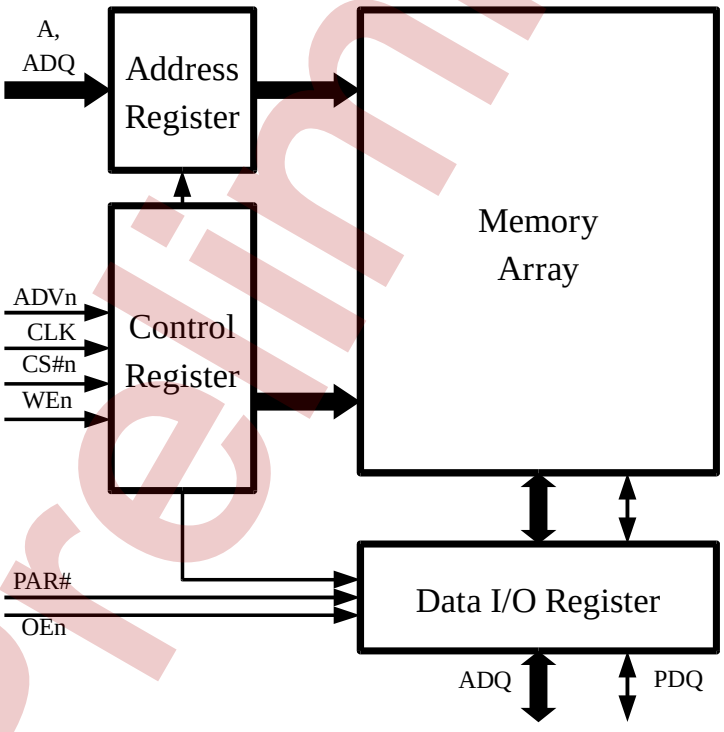


Figure 1: Block Diagram

DESCRIPTION

The RC2103209 is a synchronous 32Kx9 RAM. The part uses a multiplexed bus (address and data). Ninth bit or parity is selected by pin configuration.

Fifteen bits of address are provided during the address cycle. Eight bits of data plus parity are transferred in the data cycle.

Parity Configuration

The ninth data bit (on the PDQ pin) is configured for data or parity by the PAR0 through PAR2 pins. These pins should all be tied high or low as required by the application. Table 1 shows the available configurations.

Table 1: Parity Selections

PAR[2:0]	Parity Bit
000	Z
001	Data Bit 9
010	Even Parity
011	Odd Parity
1xx	Parity Error

Parity Mode 000

The PDQ parity bit is not used. The user should tie the PDQ pin to GND if this mode is used.

Parity Mode 001

The PDQ parity bit is a ninth data bit. Read/write operations are used.

Parity Mode 010

The PDQ parity bit is an even parity bit. When data is written to the memory, the even parity of the eight data bits is calculated and stored in memory. When a read occurs, the even parity bit is output on the PDQ pin.

Parity Mode 011

The PDQ parity bit is an odd parity bit. When data is written to the memory, the odd parity of the eight data bits is calculated and stored in memory. When a read occurs, the odd parity bit is output on the PDQ pin.

Parity Mode 1xx

The PDQ parity bit is an error flag. When data is written to the memory, the parity of the eight data bits is calculated and stored in memory. When a read occurs, the stored bit is compared to the parity of the eight read bits. If there is a parity error, the PDQ pin is asserted (high). Otherwise, the PDQ pin remains low.

Read

Read occurs when WEn is not asserted, and an address cycle starts (see Figure 2). During the address cycle, the address is issued to the part. One the next cycle, the read data is available.

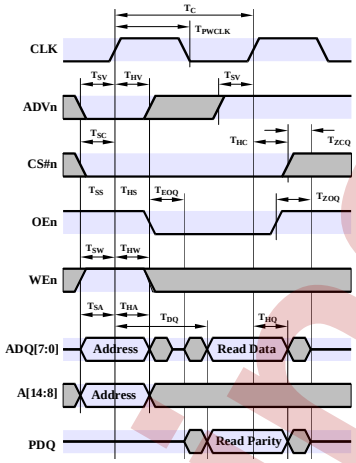


Figure 2: Read Operation

Write

Write occurs when WEn is asserted, and an address cycle starts (see Figure 2). During the address cycle, the address is issued to the part. One the next cycle, the write data is issued.

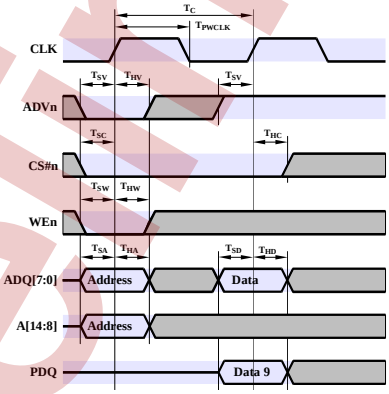


Figure 3: Write Operation

SPECIFICATIONS

Absolute Maximums (1)

Temperature ..... -55 to 350ºC
Power Supply (V_{DD} referenced to ground) ..... -0.2 to 6.0 volts
Battery Voltage (V_{DDB} referenced to ground) ..... -0.2 to 6.0 volts
IO Voltage (referenced to ground) ..... -0.2 to 6.0 volts

Operating Conditions

Temperature (die temperature) ..... -55 to 300ºC
Power Supply (V_{DD} referenced to ground) ..... 4.5 to 5.5 volts
Battery Voltage (V_{DDB} referenced to ground) ..... 3.4 to (V_{DD}-0.1) volts
IO Voltage (referenced to ground) ..... 0.2 to (V_{DD}+0.2) volts

1. Exceeding the absolute maximum specifications may cause permanent damage to the part

DC Characteristics

Table 2: DC Characteristics

Symbol	Description	Min	Typ	Max @225C	Max @300C	Unit	Note
T	Temperature	-55	25	225	300	ºC	
V_{DD}	Digital Power Supply	4.5	5	5.5	5.5	V	
V_{DDB}	Battery Power Supply	3.4		V_{DD}-0.1	V_{DD}-0.1	V	1
I_{DD}	Active Current			2.5	3	mA/MHz	2
I_{DD}	Standby Current (CSn = V_{DD})			1.5	2	mA/MHz	2,3
I_{DDB}	Battery Current (V_{DD}=0)			0.005	8	mA	4
V_{OH}	Output High Voltage (I_{OH}=2mA)	0.9*V_{DD}				V	
V_{OL}	Output Low Voltage (I_{OL}=2mA)			0.5	0.5	V	
V_{IH}	Input High Voltage	0.8*V_{DD}				V	
V_{IL}	Input Low Voltage			1.0	1.0	V	
I_I	Input Current			10	10	uA	

Notes:

1. For systems not using battery backup, connect the V_{DDB} pin to GND.
2. No Output Load.
3. All bus signals toggling simulating other memories on the bus.
4. When not running on the battery, this DC current must be added to active and standby currents.

AC Characteristics

Table 3: AC Characteristics

Symbol	Description	Min	Max @225C	Max @300C	Unit	Note
F	Frequency		10	8	MHz	
T_{PWCLK}	Pulse Width: CLK	45			nS	
T_{DO}	Delay: CLK ↑ to Q		75	80	nS	
T_{HO}	Hold: Q after CLK ↑	TBD	TBD	TBD	nS	
T_{EOO}	Enable: OEn ↓ to Q	TBD	TBD	TBD	nS	
T_{ZCO}	Disable: CSn ↑ to Q	TBD	TBD	TBD	nS	
T_{ZOO}	Disable: OEn ↑ Q	TBD	TBD	TBD	nS	
T_{SA}	Setup: Address to CLK ↑	TBD			nS	
T_{SC}	Setup: CSn ↓ to CLK ↑	65			nS	
T_{SD}	Setup: Data to CLK ↑	TBD			nS	
T_{SV}	Setup: ADVn ↓ to CLK ↑	5			nS	
T_{SW}	Setup: WEn to CLK ↑	8			nS	
T_{HA}	Hold: Address CLK ↑	TBD			nS	
T_{HC}	Hold: CSn ↑ from CLK ↑	0			nS	
T_{HD}	Hold: Data from CLK ↑	TBD			nS	
T_{HV}	Hold: ADVn ↑ from CLK ↑	2			nS	
T_{HW}	Hold: WEn from CLK ↑	0			nS	
T_{PWR}	Rise: V_{DD}	1			mS	1
T_{PWF}	Fall: V_{DD}	0			nS	1

Notes:

1. Sampled Only

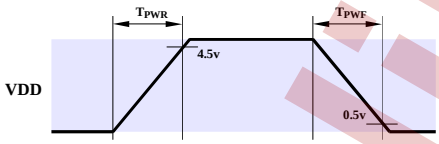


Figure 4: Power Supply Ramp

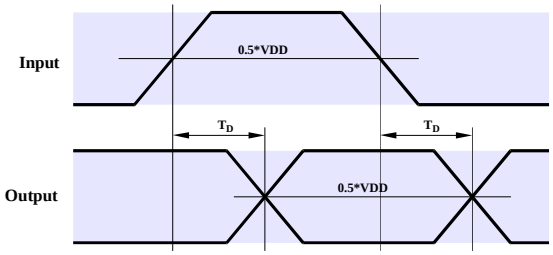


Figure 5: Delay Measurement

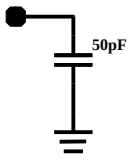


Figure 6: AC Measurement Load

PACKAGING

The RC2103209 is packaged in a 68 pin J-Lead QFP.

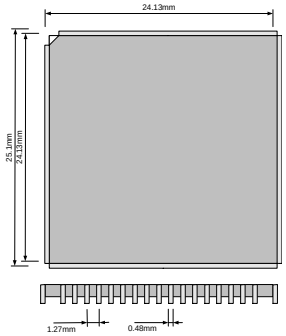


Table 4: Pin Out

Pin	Name	Dir	Function	Pin	Name	Dir	Function
1	GND	Ground	Ground	35	GND	Ground	Ground
2	ADQ3	IO	Address/Data	36	A13	Input	Address Input
3	nc	na	No Connection	37	nc	na	No Connection
4	ADQ5	IO	Address/Data	38	CS1n	Input	Chip Enable (low active)
5	nc	na	No Connection	39	nc	na	No Connection
6	ADQ7	IO	Address/Data	40	nc	na	No Connection
7	ADVn	Input	Address Valid (low active)	41	CLK	Input	Clock
8	nc	na	No Connection	42	nc	na	No Connection
9	VDD	Power	Power Supply	43	VDD	Power	Power Supply
10	GND	Ground	Ground	44	GND	Ground	Ground
11	nc	na	No Connection	45	nc	na	No Connection
12	OEn	Input	Output Enable (low active)	46	ADQ6	IO	Address/Data
13	nc	na	No Connection	47	nc	na	No Connection
14	CS0n	Input	Chip Enable (low active)	48	ADQ4	IO	Address/Data
15	nc	na	No Connection	49	nc	na	No Connection
16	A14	Input	Address Input	50	ADQ2	IO	Address/Data
17	VDD	Power	Power Supply	51	VDD	Power	Power Supply
18	GND	Ground	Ground	52	GND	Ground	Ground
19	A12	Input	Address Input	53	WEn	Input	Write Select (low active)
20	nc	na	No Connection	54	nc	na	No Connection
21	A11	Input	Address Input	55	PAR0	Input	Parity Control Select
22	nc	na	No Connection	56	nc	na	No Connection
23	A10	Input	Address Input	57	PAR1	Input	Parity Control Select
24	A9	Input	Address Input	58	VDDB	Power	Battery Backup Supply
25	nc	na	No Connection	59	nc	na	No Connection
26	VDD	Power	Power Supply	60	VDD	Power	Power Supply
27	GND	Ground	Ground	61	GND	Ground	Ground
28	nc	na	No Connection	62	nc	na	No Connection
29	A8	Input	Address Input	63	PDQ	IO	Parity
30	nc	na	No Connection	64	nc	na	No Connection
31	PAR2	Input	Parity Mode	65	ADQ0	IO	Address/Data
32	nc	na	No Connection	66	nc	na	No Connection
33	GND	Ground	Ground	67	ADQ1	IO	Address/Data
34	VDD	Power	Power Supply	68	VDD	Power	Power Supply