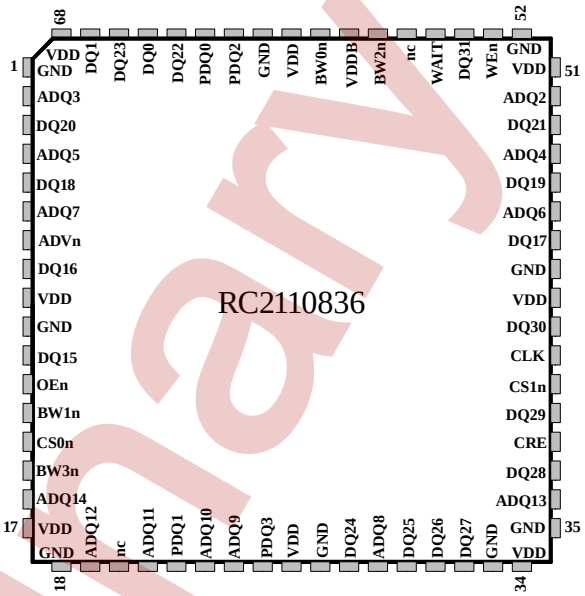
FEATURES

- 8K x 36 Random Access Memory
- 5 volt Operation
- 3.4 volt Battery Back Up
- Fully Static Design
- Wide Operating Temperature Range
- Parity and Burst Mode Options
- RC10001 Compatible



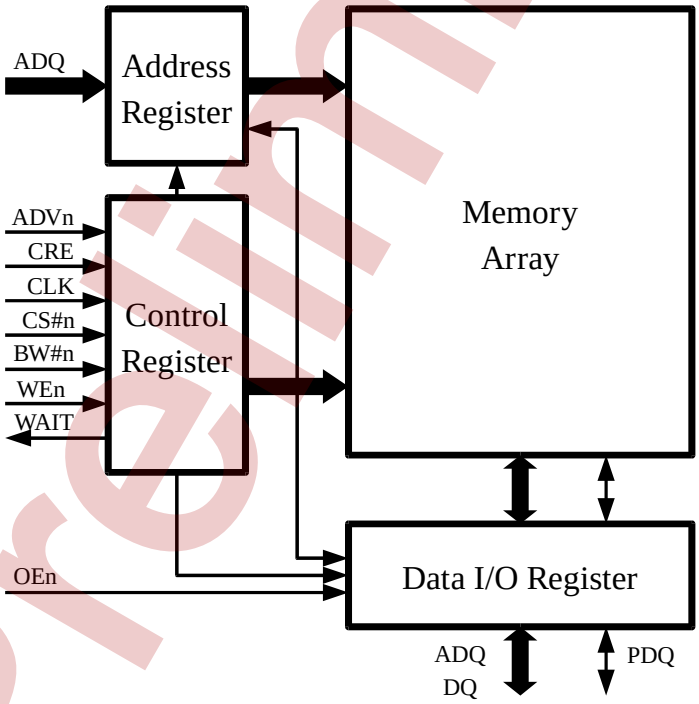


Figure 1: Block Diagram

DESCRIPTION

The RelChip™ RC2110836 is a synchronous 8Kx36 RAM compatible with the RC10001 microcontroller. The memory is highly configurable, with options for data width, parity, latency, and burst-mode. Each byte of the basic thirty two data pins can be written individually with the byte write (BW0n through BW3n) control pins.

Thirteen bits of address (ADQ[14:2]) are provided during the address cycle. The data is word aligned.

Configuration

The RC2110836 has many configuration options. The memory is thirty six bits wide, but can be configured to thirty two bits with four parity bits. The parity bits are configured even, odd, or parity error. Latency, or the number of cycles from the address cycle to the data cycle, is programmable from one to eight cycles. A single address cycle can trigger a read or write of four words in the burst mode.

Configuration Register

The configuration consists of two registers of fourteen bits (see Table 1). This allows a special single cycle write of the configuration independent of the current programmed configuration. The first register stores the latency and burst configuration, while the second stores the parity configuration.

Table 1: Configuration Register

A[14]	Bit	Symbol	Description	Default
0	13:11	Latency Count	Data Available in n+1 Clocks (See Table 2)	010
0	10:1	Reserved	Reserved	na
0	0	Burst Length	0=1, 1=4	0
1	13:3	Reserved	Reserved	na
1	2:0	Parity Selection	Parity Mode (See Table 3)	000

Latency

Latency can be programmed from one to eight cycles (see Table 1 and Table 2). Latency is the number of clock cycles from the address cycle to the data cycle (either read or write). Different latency settings are illustrated in the Example Operations section. Latency is configured with bits 13 through 11 of the first configuration register. The default value is three cycles.

Table 2: Latency Selections

Value (binary)	Latency (cycles)	default
000	1	
001	2	
010	3	X
011	4	
100	5	
101	6	
110	7	
111	8	

Burst Mode

The RC2110836 can execute one or four read or write operations for each address cycle. This mode is set in the configuration register (see Table 1). Burst operations begin at the address specified during the address cycle. Subsequent operations occur at the next address (modulo 4). If the operation is started with A[3:2] set to “00,” the part will use that address for the first operation, followed by “01,” “10,” and “11.” However, if the operations begin at A[3:2] equal to “10,” the sequence would then follow as “11,” “00,” and “01.” This operation will not modify A[4]. A burst operation is aborted or ended by deselecting the part (CS0n or CS1n go high for one clock edge). An abort will not roll-back previous write operations. A burst will continue (with address wrapping) until the part is deselected.

Parity

The parity IO is configured through bits 2:0 in the configuration register (see Table 1 and Table 3). The parity IO pins can be configured to floating, data, parity, or parity error. If they are not used, the pins should be configured to float, and be tied to ground externally.

The RC2110836 can be configured as a by thirty two bit part with parity, or as a by thirty six bit part without. As a thirty two bit part, the parity IO pins are byte parity pins for the four bytes in a word. For thirty six bit operation, the parity IO pins (PDQ0 through PDQ3) are used for data.

The RC2110836 will calculate the parity for each written byte (D[7:0], D[15:8], D[23:16], and D[31:24]), storing the values in the parity bits (P[0] through P[3] respectively). The parity is determined by the mode. For even or odd parity modes, the four bits are calculated and stored in memory. The parity error mode performs the same during a write.

If the part is read in even or odd parity modes, the parity value calculated during the write is reported on the PDQ pins. Thus, any bit disturbance while stored would be represented on the PDQ pins.

If the part is read in the parity error mode, the four bytes read have a new parity calculated. The PDQ pin is asserted when this new parity value is different than the stored one.

Table 3: Parity Selections

Value (binary)	Parity Bit (PDQ)	default
000	Z	
001	Nine Bit Data	X
010	Even Parity	
011	Odd Parity	
1xx	Parity Error	

Status Register

There are, like the configuration register, two status registers. These are full thirty-two bit registers (see Table 4). The status includes all the configuration bits plus product identification fields.

Table 4: Status Register Contents

A[14]	Register	Symbol	Description	Constant
0	31:14	Reserved	Reserved	0
0	13:11	Latency Count	Data Available in n+1 Clocks (See Table 2)	
0	10:1	Reserved	Reserved	1010100
0	0	Burst Length	0=1, 1=4	
1	31:16	Part Number	Integer	ROM
1	15:14	Reserved	Reserved	00
1	13:10	Configuration	Integer	0101
1	9:3	Revision Number	Integer	ROM
1	2:0	Parity Selection	Parity Mode (See Table 3)	

Configuration Write

Configuration writes always occur in a single cycle. With the Configuration Register Enable pin (CRE) asserted high, a write operation is initiated (see Figure 2). Address input 14 selects which of the two configuration registers is addressed. Address inputs 13 through 0 set the configuration bits.

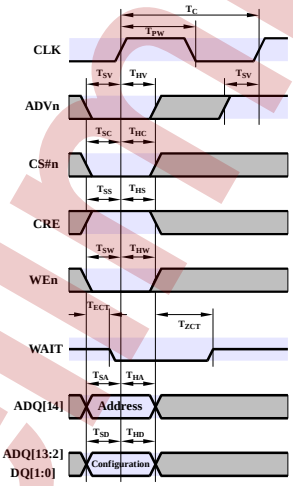


Figure 2: Configuration Write

Status Read

A status read is identical to a normal read except that the CRE pin is asserted high (see Figure 3). The parity bit is always output as a low during a status read if enabled.

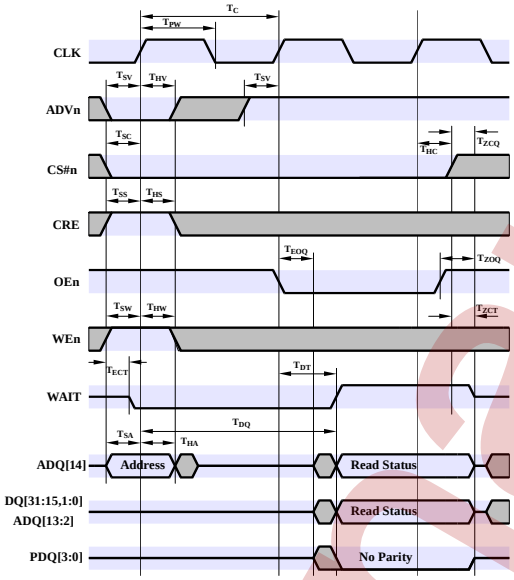


Figure 3: Status Read: 2 Cycle Latency

Example Operations

Simple Read and Write

Simple single read and write operations with one cycle latency are shown in Figure 4 and Figure 5. Read and write in this mode is just issues the address in one cycle and performs the operation in the next. Note that the byte write pins (BW0n through BW3n) select the byte(s) to write. BW0n selects D[7:0], BW1n selects D[15:8], BW2n selects D[23:16], and BW3n selects D[31:24].

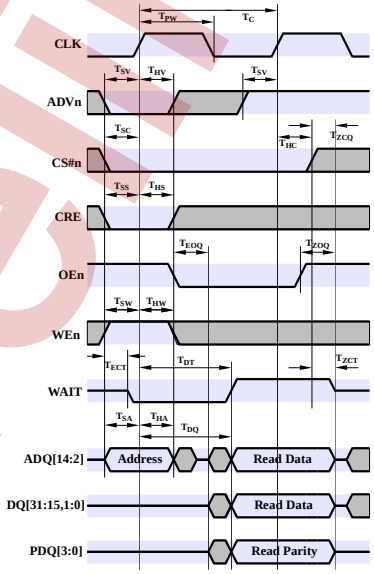


Figure 4: Simple Read: No Burst, 1 Cycle Latency

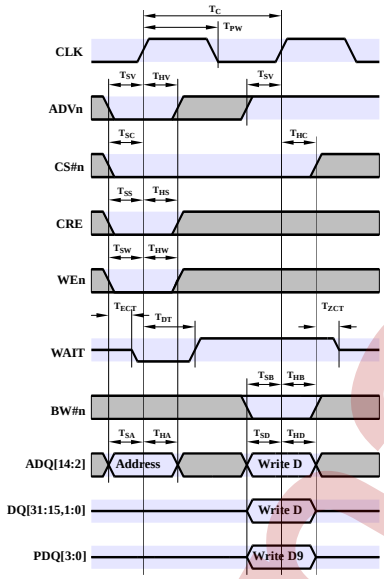


Figure 5: Simple Write: No Burst, 1 Cycle Latency

Burst Mode Read and Write

Burst mode read/write operations are shown in Figure 6 through Figure 9. Read and write in this mode is issues the address in one cycle, and then sequentially reads or writes four locations. The byte write pins control the bytes to write. Address arithmetic takes A[3:2], increments it modulo 4 for each internal operation. Thus, the operation wraps around the four addresses.

The burst mode operation ends when the chip select is deasserted (CS0n and/or CS1n).

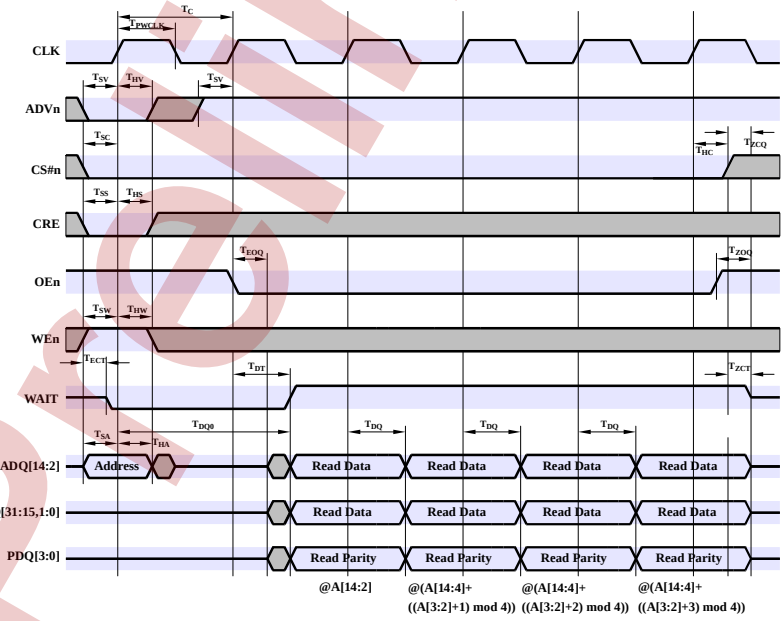


Figure 6: Data Read: Burst Mode, 2 Cycle Latency

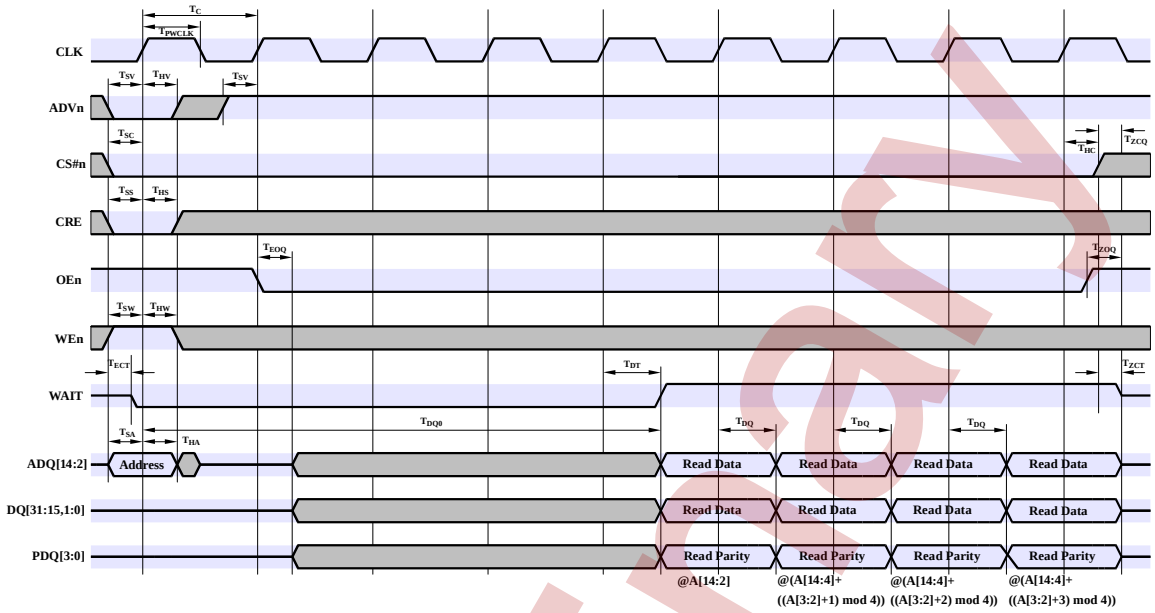


Figure 7: Data Read: Burst Mode, 5 Cycle Latency

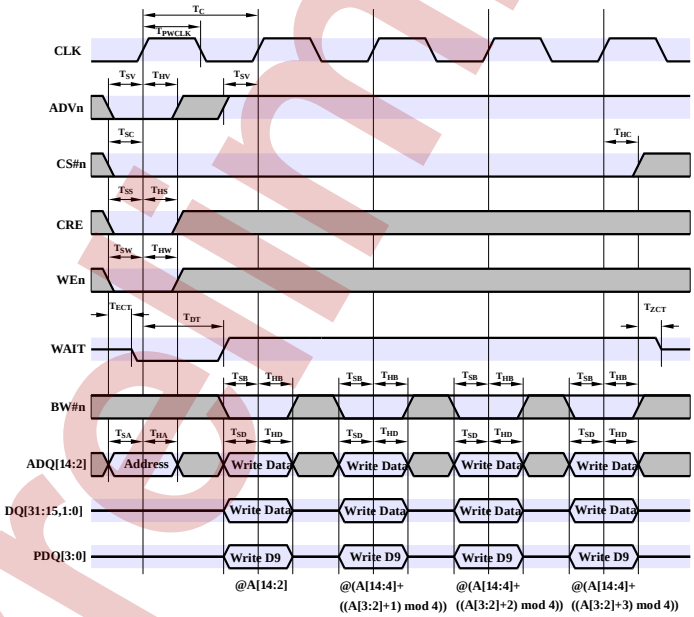


Figure 8: Data Write: Burst Mode, 1 Cycle Latency

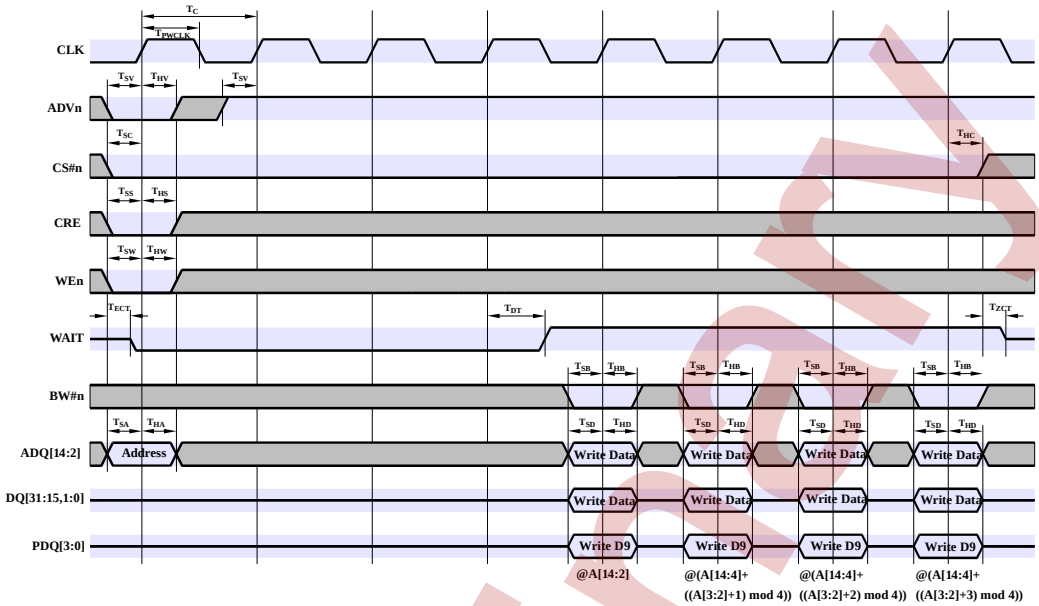


Figure 9: Data Write: Burst Mode, 4 Cycle Latency

Read and Write with Latency

Adding latency to operations, whether burst mode or not, just adds cycles between the address cycle and the first operation cycle. The examples of Figure 6 through Figure 9 show various latency delays in read and write operations.

SPECIFICATIONS

Absolute Maximums (1)

Temperature ..... -55 to 350ºC
Power Supply (V_{DD} referenced to ground) ..... -0.2 to 6.0 volts
Battery Voltage (V_{DDB} referenced to ground) ..... -0.2 to 6.0 volts
IO Voltage (referenced to ground) ..... -0.2 to 6.0 volts

Operating Conditions

Temperature (die temperature) ..... -55 to 300ºC
Power Supply (V_{DD} referenced to ground) ..... 4.5 to 5.5 volts
Battery Voltage (V_{DDB} referenced to ground) ..... 3.4 to (V_{DD}-0.1) volts
IO Voltage (referenced to ground) ..... -0.2 to (V_{DD}+0.2) volts

1. Exceeding the maximum specifications may cause permanent damage

DC Characteristics

Table 5: DC Characteristics

Symbol	Description	Min	Typ	Max @225C	Max @300C	Unit	Note
T	Temperature	-55	25	225	300	ºC	
V_{DD}	Digital Power Supply	4.5	5	5.5	5.5	V	
V_{DDB}	Battery Power Supply	3.4		V_{DD}-0.1	V_{DD}-0.1	V	1
I_{DD}	Active Current			2.5	3	mA/MHz	2
I_{DDS}	Standby Current (CSn=V_{DD})			1.5	2	mA/MHz	2,3
I_{DDB}	Battery Current (V_{DD}=0)			0.005	8	mA	4
V_{OH}	Digital Output High Voltage (I_{OH}=2mA)	0.9*V_{DD}				V	
V_{OL}	Digital Output Low Voltage (I_{OL}=2mA)			0.5		V	
V_{IH}	Digital Input High Voltage	0.8*V_{DD}				V	
V_{IL}	Digital Input Low Voltage			1.0		V	
I_I	Digital Input Current			10		uA	

Notes:

1. For systems not using battery backup, connect V_{DDB} to GND.
2. No Output Load.
3. All bus signals toggling simulating other memories on the bus.
4. When not running on the battery, this DC current must be added to active and standby currents.

AC Characteristics

Table 6: AC Characteristics

Symbol	Description	Min	Max @225C	Max @300C	Unit	Note
F	Frequency		10	8	MHz	
T_{PW}	Pulse Width: CLK	45			nS	
T_{DO}	Delay: Q from CLK ↑		75	80	nS	
T_{DT}	Delay: CLK ↑ to WAIT		45	50	nS	
T_{HO}	Hold: Q after CLK ↑	TBD	TBD	TBD	nS	
T_{ECT}	Enable: CSn ↓ to WAIT	TBD	TBD	TBD	nS	
T_{EOQ}	Enable: OEn ↓ to Q	TBD	TBD	TBD	nS	
T_{ZCQ}	Disable: CSn ↑ to Q	TBD	TBD	TBD	nS	
T_{ZCT}	Disable: CSn ↑ to WAIT	TBD	TBD	TBD	nS	
T_{ZOQ}	Disable: OEn ↑ to Q	TBD	TBD	TBD	nS	
T_{SA}	Setup: Address to CLK ↑	TBD			nS	
T_{SB}	Setup: BW#n to CLK ↑	TBD			nS	
T_{SC}	Setup: CSn ↓ to CLK ↑	65			nS	
T_{SD}	Setup: Data to CLK ↑	TBD			nS	
T_{SS}	Setup: CRE to CLK ↑	8			nS	
T_{SV}	Setup: ADVn ↓ to CLK ↑	5			nS	
T_{SW}	Setup: WEn to CLK ↑	8			nS	
T_{HA}	Hold: Address from CLK ↑	TBD			nS	
T_{HB}	Hold: BW#n from CLK ↑	TBD			nS	
T_{HC}	Hold: CSn ↑ from CLK ↑	0			nS	
T_{HD}	Hold: Data from CLK ↑	TBD			nS	
T_{HS}	Hold: CRE from CLK ↑	0			nS	
T_{HV}	Hold: ADVn ↑ from CLK ↑	2			nS	
T_{HW}	Hold: WEn from CLK ↑	0			nS	
T_{PWR}	Rise: V_{DD}	1			mS	1
T_{PWF}	Fall: V_{DD}	0			nS	1

Notes:

1. Sampled Only

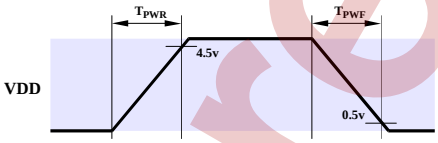


Figure 10: Power Supply Ramp

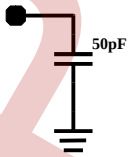


Figure 11: AC Measurement Load

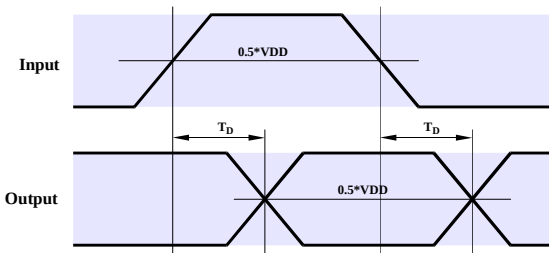


Figure 12: Delay Measurement

PACKAGING

The RC2110836 is packaged in a 68 pin J-Lead Ceramic QFP.

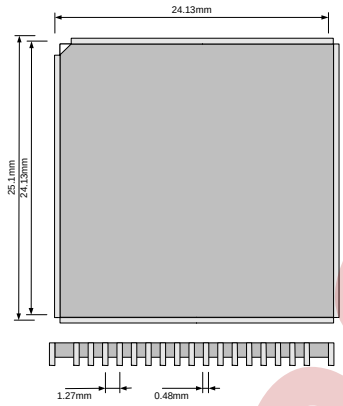


Table 7: Pin Out

Pin	Name	Dir	Function	Pin	Name	Dir	Function
1	GND	Ground	Ground	35	GND	Ground	Ground
2	ADQ3	I/O	Address/Data IO	36	ADQ13	I/O	Address/Data IO
3	DQ20	I/O	Data IO	37	DQ28	I/O	Data IO
4	ADQ5	I/O	Address/Data IO	38	CRE	Input	Control Register Enable
5	DQ18	I/O	Data IO	39	DQ29	I/O	Data IO
6	ADQ7	I/O	Address/Data IO	40	CS1n	Input	Chip Enable (low active)
7	ADVn	Input	Address Available (low active)	41	CLK	Input	Clock
8	DQ16	I/O	Data IO	42	DQ30	I/O	Data IO
9	VDD	Power	Power Supply	43	VDD	Power	Power Supply
10	GND	Ground	Ground	44	GND	Ground	Ground
11	DQ15	I/O	Data IO	45	DQ17	I/O	Data IO
12	OEn	Input	Output Enable (low active)	46	ADQ6	I/O	Address/Data IO
13	BW1n	Input	Byte 1 Write Enable (low active)	47	DQ19	I/O	Data IO
14	CS0n	Input	Chip Enable (low active)	48	ADQ4	I/O	Address/Data IO
15	BW3n	Input	MSB Write Enable (low active)	49	DQ21	I/O	Data IO
16	ADQ14	I/O	Address/Data IO	50	ADQ2	I/O	Address/Data IO
17	VDD	Power	Power Supply	51	VDD	Power	Power Supply
18	GND	Ground	Ground	52	GND	Ground	Ground
19	ADQ12	I/O	Address/Data IO	53	WEn	Input	Data Write Enable (low active)
20	nc	na	Not Connected	54	DQ31	I/O	Data IO
21	ADQ11	I/O	Address/Data IO	55	WAIT	Output	Data Available (low = wait)
22	PDQ1	I/O	Byte 1 Parity	56	nc	na	Not Connected
23	ADQ10	I/O	Address/Data IO	57	BW2n	Input	Byte 2 Write Enable (low active)
24	ADQ9	I/O	Address/Data IO	58	VDDB	Power	Battery Backup Supply
25	PDQ3	I/O	MSB Parity	59	BW0n	Input	LSB Write Enable (low active)
26	VDD	Power	Power Supply	60	VDD	Power	Power Supply
27	GND	Ground	Ground	61	GND	Ground	Ground
28	DQ24	I/O	Data IO	62	PDQ2	I/O	Byte 2 Parity
29	ADQ8	I/O	Address/Data IO	63	PDQ0	I/O	LSB Parity
30	DQ25	I/O	Data IO	64	DQ22	I/O	Data IO
31	DQ26	I/O	Data IO	65	DQ0	I/O	Data IO
32	DQ27	I/O	Data IO	66	DQ23	I/O	Data IO
33	GND	Ground	Ground	67	DQ1	I/O	Data IO
34	VDD	Power	Power Supply	68	VDD	Power	Power Supply