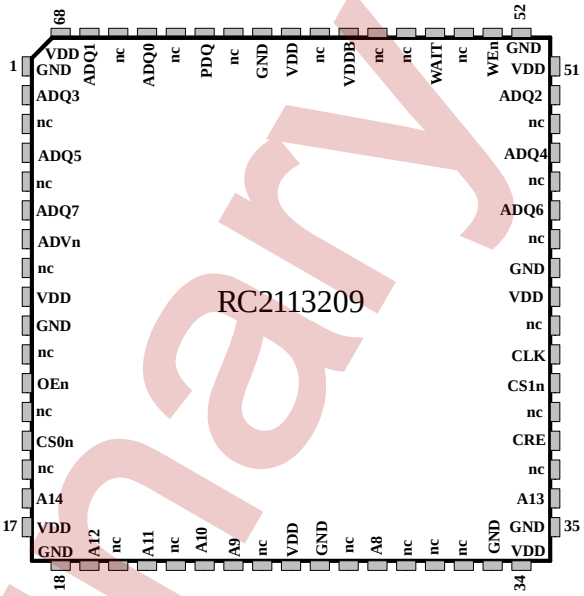
FEATURES

- 32K x 9 Random Access Memory
- 5 volt Operation
- 3.4 volt Battery Back Up
- Fully Static Design
- Wide Operating Temperature Range
- Parity and Burst Mode Options
- RC10001 Compatible



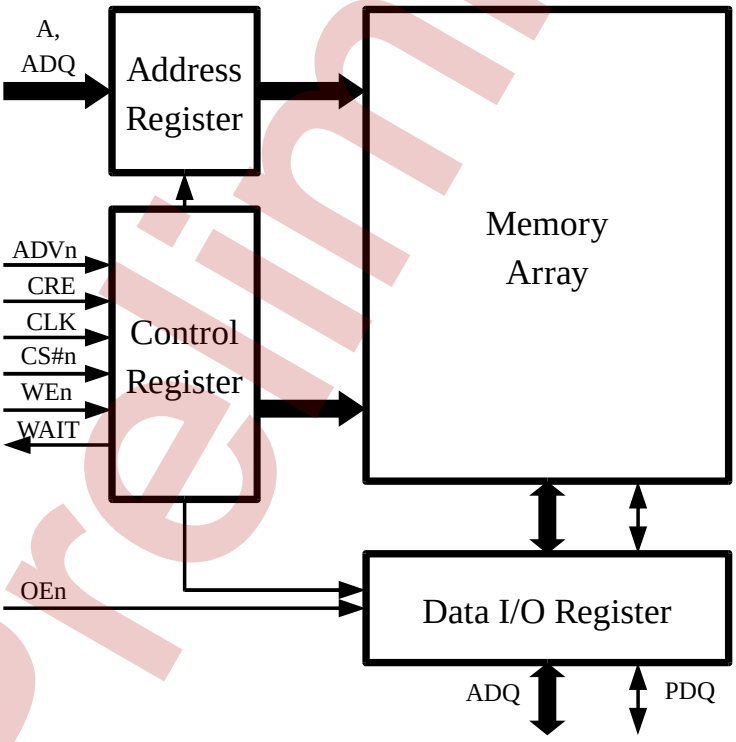


Figure 1: Block Diagram

DESCRIPTION

Configuration

The RC2113209 has many configuration options. The memory is nine bits wide, but can be configured to eight bits plus parity. The parity bit is configured even, odd, or parity error. Latency, or the number of cycles from the address cycle to the data cycle, is programmable from one to eight cycles. A single address cycle can trigger a read or write of four bytes in the burst mode.

Configuration Register

The configuration consists of two registers of fourteen bits (see Table 1). This allows a special single cycle write of the configuration independent of the current programmed configuration. The first register stores the latency and burst configuration, while the second stores the parity configuration.

Table 1: Configuration Register

A[14]	Bit	Symbol	Description	Default
0	13:11	Latency Count	Data Available in n+1 Clocks (See Table 2)	010
0	10:1	Reserved	Reserved	na
0	0	Burst Length	0=1, 1=4	1
1	13:3	Reserved	Reserved	na
1	2:0	Parity Selection	Parity Mode (See Table 3)	0

Latency

Latency can be programmed from one to eight cycles (see Table 1 and Table 2). Latency is the number of clock cycles from the address cycle to the data cycle (either read or write). Different latency settings are illustrated in the Example Operations section. Latency is configured with bits 13 through 11 of the first configuration register. The default value is three cycles.

Table 2: Latency Selections

Value (binary)	Latency (cycles)	default
000	1	
001	2	
010	3	X
011	4	
100	5	
101	6	
110	7	
111	8	

Burst Mode

The RC2113209 can execute one or four read or write operations for each address cycle. This mode is set in the configuration register (see Table 1). Burst operations begin at the address specified during the address cycle. Subsequent operations occur at the next address (modulo 4). If the operation is started with A[1:0] set to “00,” the part will use that address for the first operation, followed by “01,” “10,” and “11.” However, if the operations begin at A[1:0] equal to “10,” the sequence would then follow as “11,” “00,” and “01.” This operation will not modify A[2]. A burst operation is aborted by deselecting the part (CS0n or CS1n go high). An abort will not roll-back previous write operations.

Parity

The parity IO is configured through bits 2:0 in the configuration register (see Table 1 and Error! Reference source not found.). This IO pin can be configured to floating, data, parity, or parity error. If it is not used, the PDQ pin should be configured to float, and be tied to ground externally.

The RC2113209 can be configured as a by eight bit part with parity, or as a by nine bit part without. As an eight bit part, the parity IO pin (PDQ) is the parity pin for the data. For nine bit operation, the parity IO pin is the ninth bit.

The RC2113209 will calculate the parity for each written byte, storing the value in the parity bit. The parity calculated is determined by the parity mode. For even or odd parity modes, the bit is calculated and stored in memory. The parity error mode will perform exactly like the fixed parity modes with the bit being stored.

If the part is read in even or odd parity modes, the parity value calculated during the write is reported on the PDQ pin. Thus, any bit disturbance while stored would be represented on the PDQ pin.

If the part is read in the parity error mode, the byte read has a new parity calculated. The PDQ pin is asserted when this new parity value is different than the stored one.

Table 3: Parity Selections

Value (binary)	Parity Bit	default
000	Z	
001	Data Bit 9	X
010	Even Parity	
011	Odd Parity	
1xx	Parity Error	

Status Register

There are, like the configuration register, two status registers. These are full thirty-two bit registers (see Table 4). The status includes all the configuration bits plus product identification fields.

Table 4: Status Register Contents

A[14]	A[1:0]	Bit	Register	Symbol	Description	Constant
0	11	7:0	31:24	Reserved	Reserved	0
0	10	7:0	23:16	Reserved	Reserved	0
0	01	7:6	15:14	Reserved	Reserved	0
0	01	5:3	13:11	Latency Count	Data Available in n+1 Clocks (See Table 2)	
0	01	2:0	10:8	Reserved	Reserved	101
0	00	7:1	7:1	Reserved	Reserved	0100000
0	00	0	0	Burst Length	0=1, 1=4	
1	11	7:0	31:24	Part Number	Integer	ROM
1	10	7:0	23:16	Part Number	Integer	ROM
1	01	7:6	15:14	Reserved	Reserved	00
1	01	5:2	13:10	Configuration	Integer	0101
1	01	1:0	9:8	Revision Number	Integer 0-127	ROM
1	00	7:3	7:3	Revision Number	Integer 0-127	ROM
1	00	2:0	2:0	Parity Selection	Parity Mode (See Table 3)	

Configuration Write

Configuration writes always occur in a single cycle. With the Configuration Register Enable (CRE) asserted high, a write operation is initiated (see Figure 2). Address input 14 selects which of the two configuration registers is addressed. Address inputs 13 through 0 set the configuration bits.

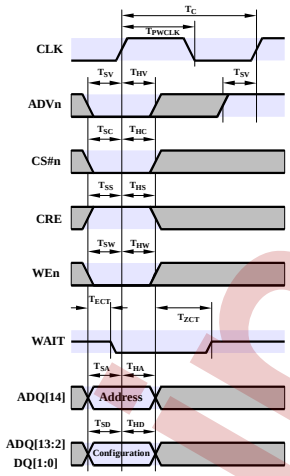


Figure 2: Configuration Write

Status Read

A status read is identical to a normal read except that the CRE pin is asserted high (see Figure 3 for an example of a burst status read). The parity bit is always output as a low during a status read if enabled.

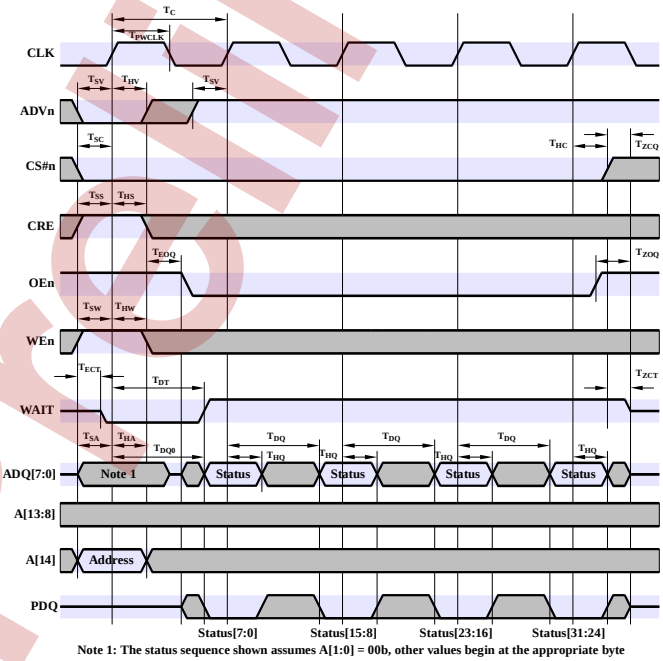


Figure 3: Status Read: Burst with 1 Cycle Latency

Example Operations

Simple Read and Write

Simple single read and write operations with one cycle latency are shown in Figure 4 and Figure 5. Read and write in this mode is just issues the address in one cycle and performs the operation in the next.

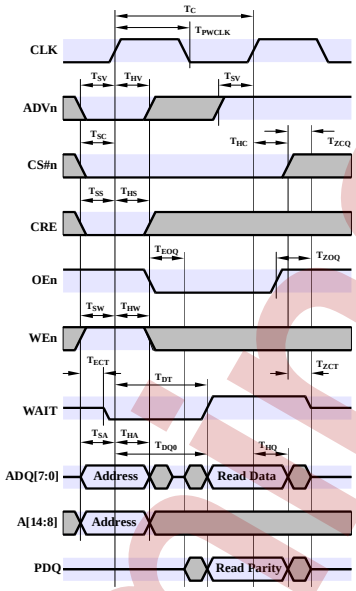


Figure 4: Simple Read: No Burst with 1 Cycle Latency

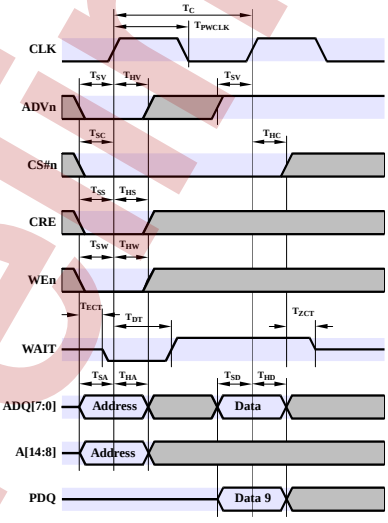


Figure 5: Simple Write: No Burst with 1 Cycle Latency

Burst Mode Read and Write

Burst mode read/write operations (single cycle latency) are shown in Figure 6 through Figure 9. Read and write in this mode is just issues the address in one cycle, and then sequentially reads the four locations. Address arithmetic takes A[1:0], increments it modulo 4 for each internal operation.

The burst mode operation ends when the chip select is deasserted (CS0n and/or CS1n).

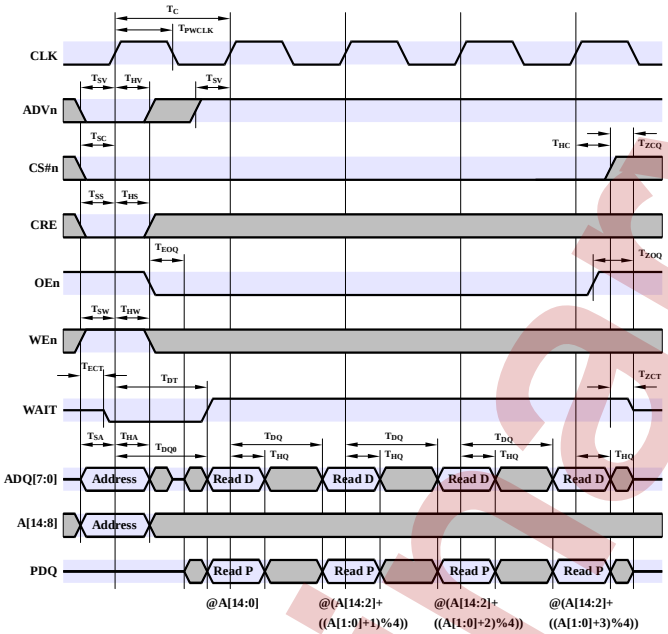


Figure 6: Data Read: Burst with 1 Cycle Latency

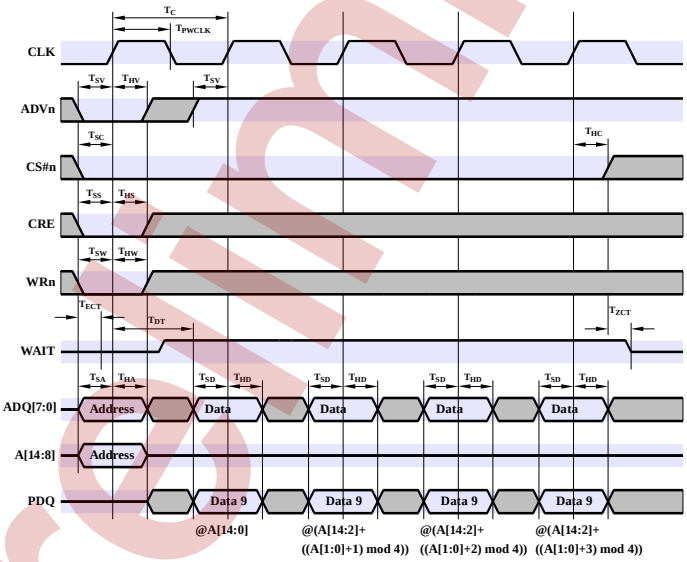


Figure 7: Data Write: Burst with 1 Cycle Latency

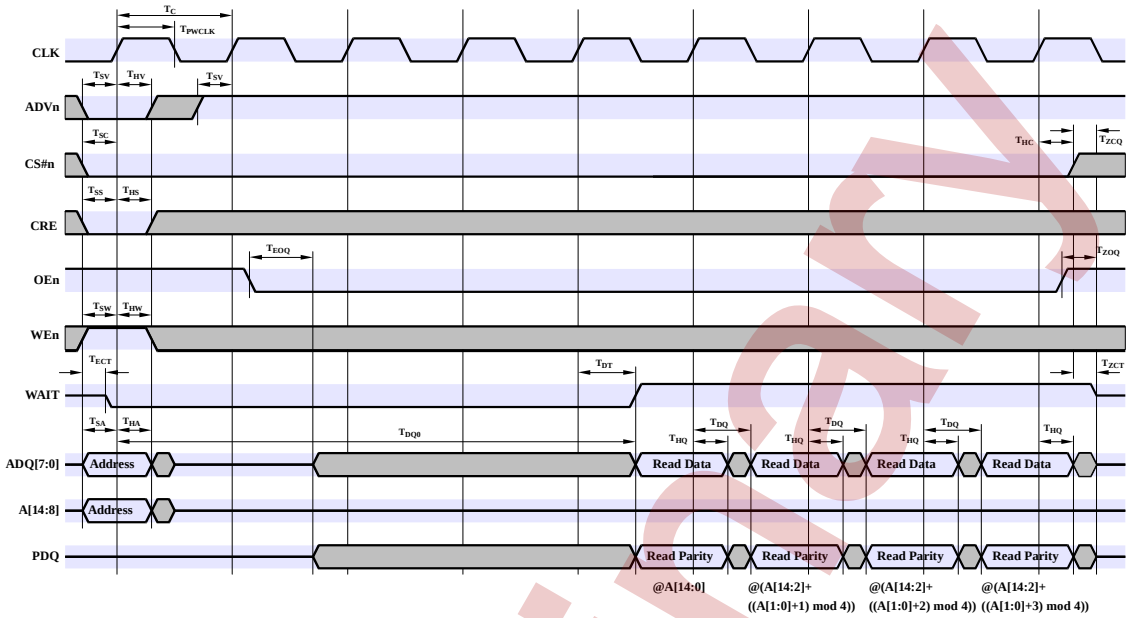


Figure 8: Data Read: Burst Mode, 5 Cycle Latency

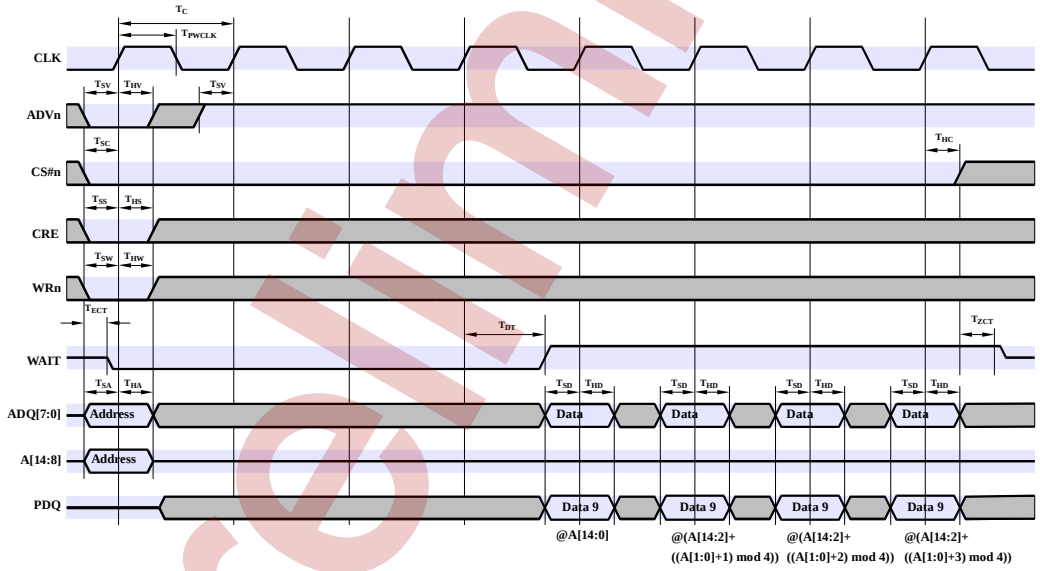


Figure 9: Data Write: Burst Mode, 4 Cycle Latency

Read and Write with Latency

Adding latency to operations, whether burst mode or not, just adds cycles between the address cycle and the first operation cycle. The examples of Error! Reference source not found. through Error! Reference source not found. show various latency delays in read and write operations.

SPECIFICATIONS

Absolute Maximums (1)

Temperature ..... -55 to 350ºC
Power Supply (V_{DD} referenced to ground)..... -0.2 to 6.0 volts
Battery Voltage (V_{DDB} referenced to ground) ..... -0.2 to 6.0 volts
IO Voltage (referenced to ground)..... -0.2 to 6.0 volts

Operating Conditions

Temperature (die temperature)..... -55 to 300ºC
Power Supply (V_{DD} referenced to ground)..... 4.5 to 5.5 volts
Battery Voltage (V_{DDB} referenced to ground) ..... 3.4 to (V_{DD}-0.1) volts
IO Voltage (referenced to ground)..... -0.2 to (V_{DD}+0.2) volts

1. Exceeding the maximum specifications may cause permanent damage to the part

DC Characteristics

Table 5: DC Characteristics

Symbol	Description	Min	Typ	Max @225C	Max @300C	Unit	Note
T	Temperature	-55	25	225	300	ºC	
V_{DD}	Digital Power Supply	4.5	5	5.5	5.5	V	
V_{DDB}	Battery Power Supply	3.4		V_{DD}-0.1	V_{DD}-0.1	V	1
I_{DD}	Active Current			2.5	3	mA/MHz	2
I_{DDS}	Standby Current (CSn=V_{DD})			1.5	2	mA/MHz	2,3
I_{DDB}	Battery Current (V_{DD}=0)			0.005	8	mA	4
V_{OH}	Digital Output High Voltage (I_{OH}=2mA)	0.9*V_{DD}				V	
V_{OL}	Digital Output Low Voltage (I_{OL}=2mA)			0.5		V	
V_{IH}	Digital Input High Voltage	0.8*V_{DD}				V	
V_{IL}	Digital Input Low Voltage			1.0		V	
I_{I}	Digital Input Current			10		uA	

Notes:

1. For systems not using battery backup, connect V_{DDB} to GND.
2. No Output Load
3. All bus signals toggling simulating other memories on the bus.
4. When not running on the battery, this DC current must be added to active and standby currents.

AC Characteristics

Table 6: AC Characteristics

Symbol	Description	Min	Max @225C	Max @300C	Unit	Note
F	Frequency		10	8	MHz	
T_{PWCLK}	Pulse Width: CLK	45			nS	
T_{DO}	Delay: CLK ↑ to Q		75	80	nS	
T_{DT}	Delay: CLK ↑ to WAIT		45	50	nS	
T_{HO}	Hold: Q after CLK ↑	TBD	TBD	TBD	nS	
T_{ECT}	Enable: CSn ↓ to WAIT	TBD	TBD	TBD	nS	
T_{EOO}	Enable: OEn ↓ to Q	TBD	TBD	TBD	nS	
T_{ZCO}	Disable: CSn ↑ to Q	TBD	TBD	TBD	nS	
T_{ZCT}	Disable: CSn ↑ to WAIT	TBD	TBD	TBD	nS	
T_{ZOO}	Disable: OEn ↑ Q	TBD	TBD	TBD	nS	
T_{SA}	Setup: Address to CLK ↑	TBD			nS	
T_{SC}	Setup: CSn ↓ to CLK ↑	65			nS	
T_{SD}	Setup: Data to CLK ↑	TBD			nS	
T_{SS}	Setup: CRE to CLK ↑	8			nS	
T_{SV}	Setup: ADVn ↓ to CLK ↑	5			nS	
T_{SW}	Setup: WEn to CLK ↑	8			nS	
T_{HA}	Hold: Address CLK ↑	TBD			nS	
T_{HC}	Hold: CSn ↑ from CLK ↑	0			nS	
T_{HD}	Hold: Data from CLK ↑	TBD			nS	
T_{HS}	Hold: CRE from CLK ↑	0			nS	
T_{HV}	Hold: ADVn ↑ from CLK ↑	2			nS	
T_{HW}	Hold: WEn from CLK ↑	0			nS	
T_{PWR}	Rise: V_{DD}	1			mS	1
T_{PWF}	Fall: V_{DD}	0			nS	1

Notes:

1. Sampled Only

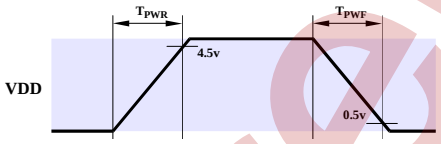


Figure 10: Power Supply Ramp

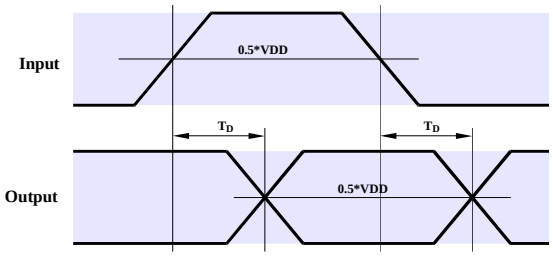


Figure 11: Delay Measurement

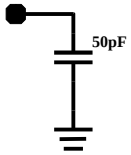


Figure 12: AC Measurement Load

PACKAGING

The RC2113209 is packaged in a 68 pin J-Lead QFP.

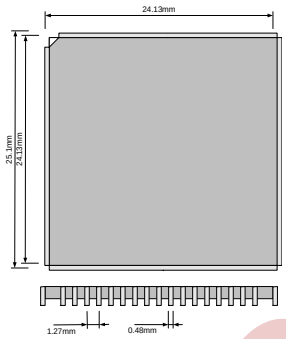


Table 7: Pin Out

Pin	Name	Dir	Function	Pin	Name	Dir	Function
1	GND	Ground	Ground	35	GND	Ground	Ground
2	ADQ3	I/O	Address/Data	36	A13	Input	Address Input
3	Nc	na	No Connection	37	nc	na	No Connection
4	ADQ5	I/O	Address/Data	38	CRE	Input	Control Register Enable
5	Nc	na	No Connection	39	nc	na	No Connection
6	ADQ7	I/O	Address/Data	40	CS1n	Input	Chip Enable (low active)
7	ADVn	Input	Address Valid (low active)	41	CLK	Input	Clock
8	Nc	na	No Connection	42	nc	na	No Connection
9	VDD	Power	Power Supply	43	VDD	Power	Power Supply
10	GND	Ground	Ground	44	GND	Ground	Ground
11	nc	na	No Connection	45	nc	na	No Connection
12	OEn	Input	Output Enable (low active)	46	ADQ6	I/O	Address/Data
13	nc	na	No Connection	47	nc	na	No Connection
14	CS0n	Input	Chip Enable (low active)	48	ADQ4	I/O	Address/Data
15	nc	na	No Connection	49	nc	na	No Connection
16	A14	Input	Address Input	50	ADQ2	I/O	Address/Data
17	VDD	Power	Power Supply	51	VDD	Power	Power Supply
18	GND	Ground	Ground	52	GND	Ground	Ground
19	A12	Input	Address Input	53	WEn	Input	Write Enable (low active)
20	nc	na	No Connection	54	nc	na	No Connection
21	A11	Input	Address Input	55	WAIT	Output	Data Valid
22	nc	na	No Connection	56	nc	na	No Connection
23	A10	Input	Address Input	57	nc	na	No Connection
24	A9	Input	Address Input	58	VDDB	Power	Battery Backup Supply
25	nc	na	No Connection	59	nc	na	No Connection
26	VDD	Power	Power Supply	60	VDD	Power	Power Supply
27	GND	Ground	Ground	61	GND	Ground	Ground
28	nc	na	No Connection	62	nc	na	No Connection
29	A8	Input	Address Input	63	PDQ	I/O	Parity
30	nc	na	No Connection	64	nc	na	No Connection
31	nc	na	No Connection	65	ADQ0	I/O	Address/Data
32	nc	na	No Connection	66	nc	na	No Connection
33	GND	Ground	Ground	67	ADQ1	I/O	Address/Data
34	VDD	Power	Power Supply	68	VDD	Power	Power Supply