

FEATURES

- 32K x 8 Random Access Memory
- 5 volt Operation
- 3.4 volt Battery Back Up
- Fully Static Design
- Wide Operating Temperature Range
- Compatible with the 8051 Interface

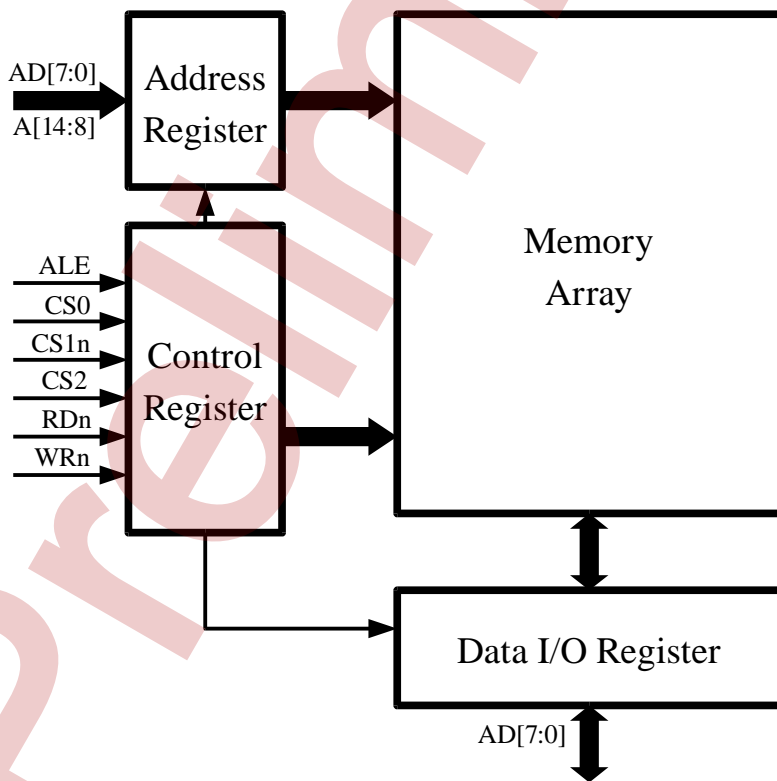
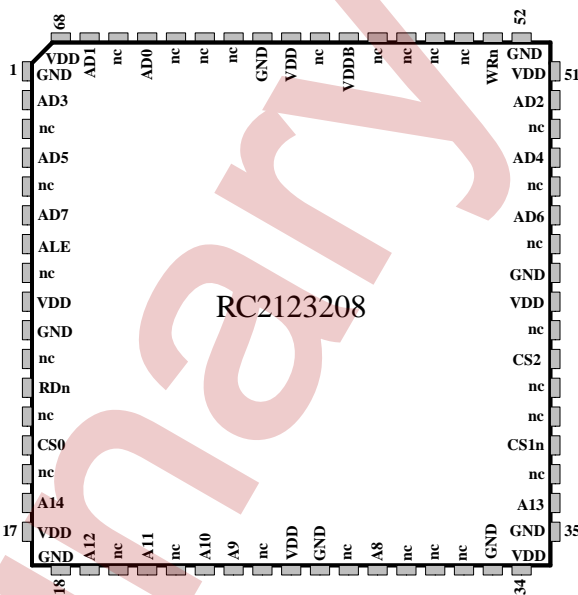


Figure 1: Block Diagram

GENERAL DESCRIPTION

The RelChip™ RC2123208 is a 32Kx8 8051-compatible RAM (256K bit). The interface is compatible with the Honeywell HT83C51 and other 8051 bus systems.

Using the PSEN/RD functions of the 8051 family, a full memory (64K program and 64K data) can be realized in just four RC2123208 ICs (see Figure 7). Chip select polarity and 8051 bus compatibility eliminate the need for extra components.

Read

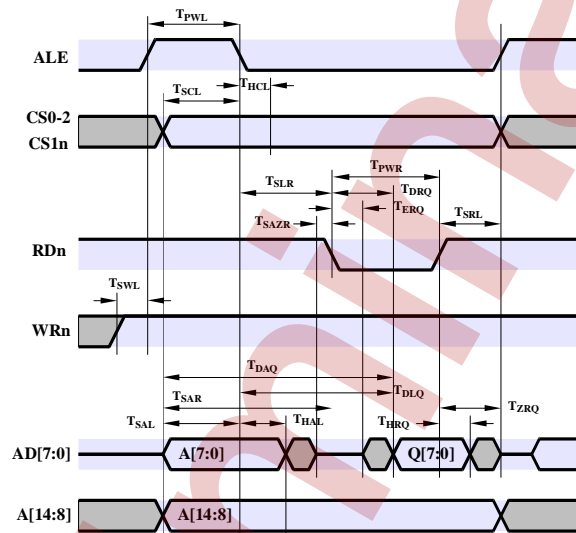


Figure 2: Read Operation

Write

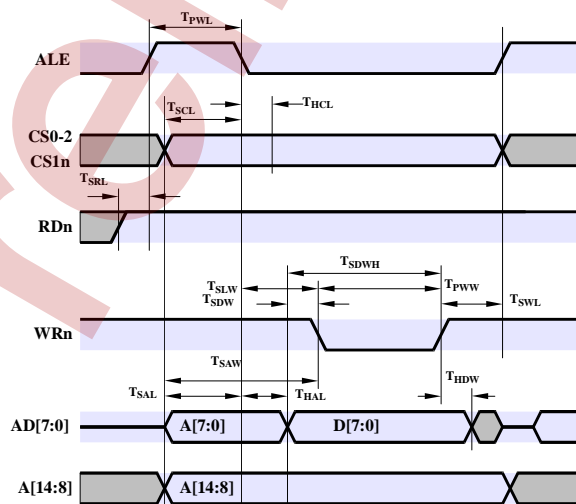


Figure 3: Write Operation

SPECIFICATIONS

Absolute Maximums (1)

Temperature	-55 to 350°C
Power Supply (V_{DD} referenced to ground).....	-0.2 to 6.0 volts
Battery Voltage (V_{DDB} referenced to ground).....	-0.2 to 6.0 volts
IO Voltage (referenced to ground).....	-0.2 to 6.0 volts

Operating Conditions

Temperature (die temperature).....	-55 to 300°C
Power Supply (V_{DD} referenced to ground).....	4.5 to 5.5 volts
Battery Voltage (V_{DDB} referenced to ground).....	3.4 to ($V_{DD}-0.1$) volts
IO Voltage (referenced to ground).....	-0.2 to ($V_{DD}+0.2$) volts

1. Exceeding the maximum specifications may cause permanent damage to the part

DC Characteristics

Table 1: DC Characteristics

Symbol	Description	Min	Typ	Max @225C	Min @300C	Unit	Note
T	Temperature	-55	25	225	300	°C	
V_{DD}	Digital Power Supply	4.5	5	5.5	5.5	V	
V_{DDB}	Battery Power Supply	3.4		$V_{DD}-0.1$	$V_{DD}-0.1$	V	1
I_{DD}	Active Current			2.5	3	mA/MHz	2
I_{DDs}	Standby Current (CS deselect)			1.5	2	mA/MHz	2,3
I_{DDB}	Battery Current ($V_{DD}=0$)			0.005	8	mA	4
V_{OH}	Digital Output High Voltage ($I_{OH}=2mA$)	$0.9*V_{DD}$				V	
V_{OL}	Digital Output Low Voltage ($I_{OL}=2mA$)			0.5		V	
V_{IH}	Digital Input High Voltage	$0.8*V_{DD}$				V	
V_{IL}	Digital Input Low Voltage			1.0		V	
I_I	Digital Input Current			10		uA	

Notes:

1. For systems not using battery backup, connect V_{DDB} to GND.
2. No Output Load.
3. All bus signals toggling simulating other memories on the bus.
4. When not running on the battery, this DC current must be added to active and standby currents.

AC Characteristics

Table 2: AC Characteristics

Symbol	Description	Min	Max @225C	Max @300C	Unit	Note
F	Frequency		10	8	MHz	
T _{PW}	Pulse Width: ALE	45			nS	
T _{PWR}	Pulse Width: RDn	45			nS	
T _{PWW}	Pulse Width: WRn	45			nS	
T _{DAO}	Delay: Q from Address		75	80	nS	
T _{DLO}	Delay: Q from ALE ↓		75	80	nS	
T _{DRO}	Delay: Q from RDn ↓		75	80	nS	
T _{HRO}	Hold: Q from RDn ↑	TBD	TBD	TBD	nS	
T _{ERO}	Enable: RDn ↓ to Q	TBD	TBD	TBD	nS	
T _{ZRO}	Disable: RDn ↑ to Q	TBD	TBD	TBD	nS	
T _{SAL}	Setup: Address to ALE ↓	TBD			nS	
T _{SAR}	Setup: Address to RDn ↓	TBD			nS	
T _{SAW}	Setup: Address to WRn ↓	TBD			nS	
T _{SAZR}	Setup: Address Float to RDn ↓	TBD			nS	
T _{SCT}	Setup: CS# to ALE ↓	TBD			nS	
T _{SDW}	Setup: Data to WRn ↓	TBD			nS	
T _{SDWH}	Setup: Data to WRn ↑	TBD			nS	
T _{SLR}	Setup: ALE ↓ to RDn ↓	TBD			nS	
T _{SLW}	Setup: ALE ↓ to WRn ↓	TBD			nS	
T _{SRI}	Setup: RDn ↑ to ALE ↑	TBD			nS	
T _{SWL}	Setup: WRn ↑ to ALE ↑	TBD			nS	
T _{HAL}	Hold: Address from ALE ↓	TBD			nS	
T _{HCL}	Hold: CS# from ALE ↓	TBD			nS	
T _{HDW}	Hold: Data from WRn ↑	TBD			nS	
T _{PWR}	Rise: V _{DD}	1			mS	1
T _{PWF}	Fall: V _{DD}	0			nS	1

Notes:

1. Sampled Only

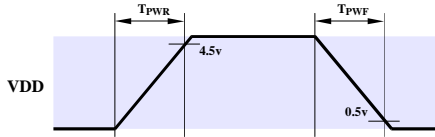


Figure 4: Power Supply Ramp

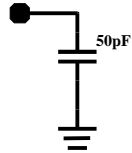


Figure 5: AC Measurement Load

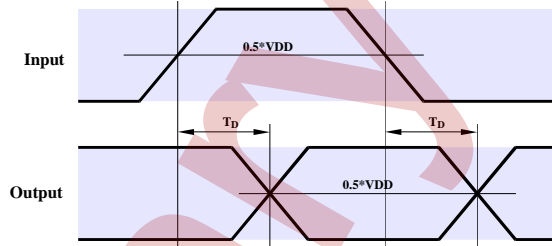


Figure 6: Delay Measurement

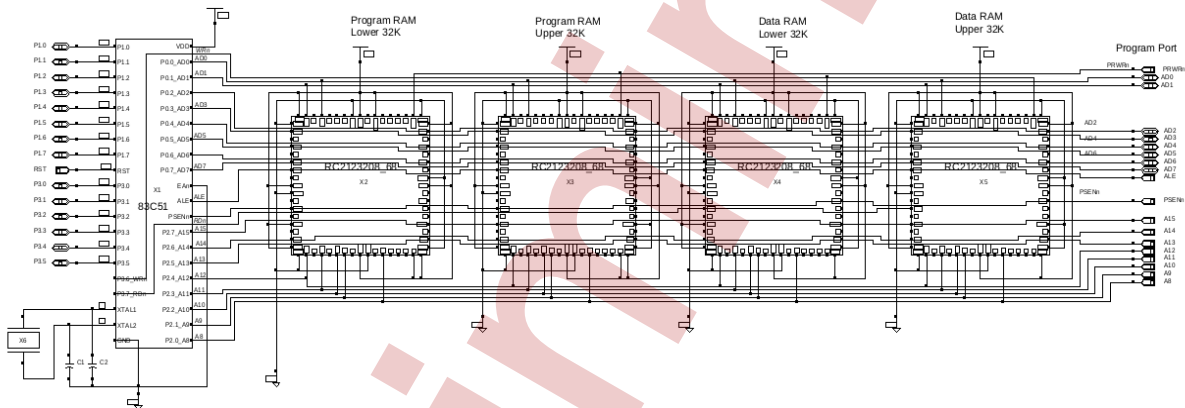


Figure 7: 83C51 Full System Schematic

PACKAGING

The RC2123208 is packaged in a 68 pin J-Lead QFP.

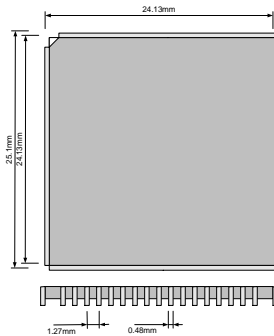


Table 3: Pin Out

Pin	Name	Dir	Function	Pin	Name	Dir	Function
1	GND	Ground	Ground	35	GND	Ground	Ground
2	AD3	I/O	Address/Data	36	A13	Input	Address Input
3	nc	na	No Connection	37	nc	na	No Connection
4	AD5	I/O	Address/Data	38	CS1n	Input	Chip Select (low active)
5	nc	na	No Connection	39	nc	na	No Connection
6	AD7	I/O	Address/Data	40	nc	na	No Connection
7	ALE	Input	Address Latch Enable	41	CS2	Input	Chip Select
8	nc	na	No Connection	42	nc	na	No Connection
9	VDD	Power	Power Supply	43	VDD	Power	Power Supply
10	GND	Ground	Ground	44	GND	Ground	Ground
11	nc	na	No Connection	45	nc	na	No Connection
12	RDn	Input	Read Enable (low active)	46	AD6	I/O	Address/Data
13	nc	na	No Connection	47	nc	na	No Connection
14	CS0	Input	Chip Select	48	AD4	I/O	Address/Data
15	nc	na	No Connection	49	nc	na	No Connection
16	A14	Input	Address Input	50	AD2	I/O	Address/Data
17	VDD	Power	Power Supply	51	VDD	Power	Power Supply
18	GND	Ground	Ground	52	GND	Ground	Ground
19	A12	Input	Address Input	53	WRn	Input	Write Enable (low active)
20	nc	na	No Connection	54	nc	na	No Connection
21	A11	Input	Address Input	55	nc	na	No Connection
22	nc	na	No Connection	56	nc	na	No Connection
23	A10	Input	Address Input	57	nc	na	No Connection
24	A9	Input	Address Input	58	VDDB	Power	Battery Backup Supply
25	nc	na	No Connection	59	nc	na	No Connection
26	VDD	Power	Power Supply	60	VDD	Power	Power Supply
27	GND	Ground	Ground	61	GND	Ground	Ground
28	nc	na	No Connection	62	nc	na	No Connection
29	A8	Input	Address Input	63	nc	na	No Connection
30	nc	na	No Connection	64	nc	na	No Connection
31	nc	na	No Connection	65	AD0	I/O	Address/Data
32	nc	na	No Connection	66	nc	na	No Connection
33	GND	Ground	Ground	67	AD1	I/O	Address/Data
34	VDD	Power	Power Supply	68	VDD	Power	Power Supply

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