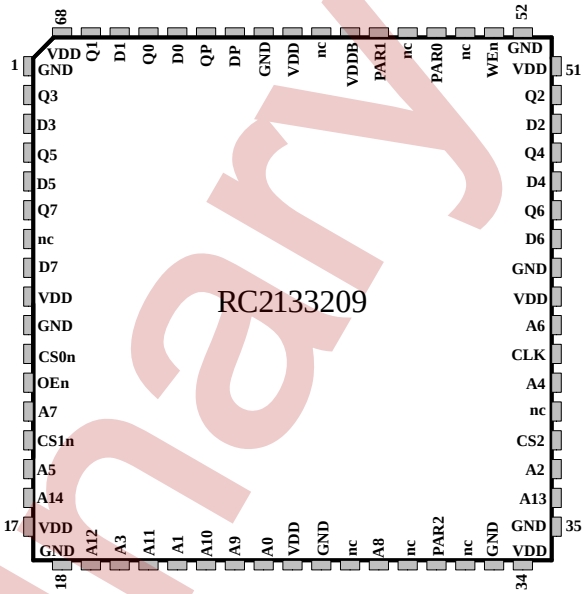
## FEATURES

- 32K x 9 Random Access Memory
- 5 volt Operation
- 3.4 volt Battery Back Up
- Fully Static Design
- Wide Operating Temperature Range
- Parity Options



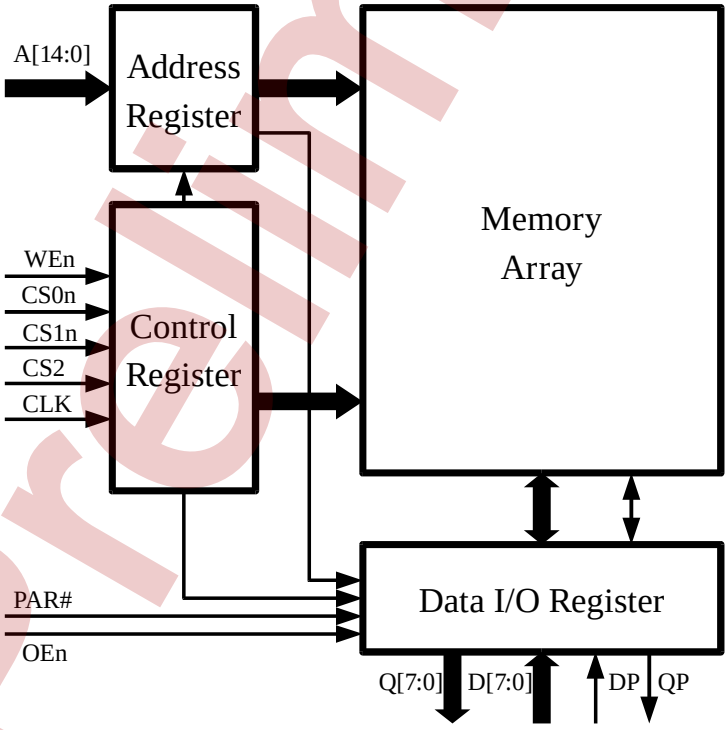




Figure 1: Block Diagram

## DESCRIPTION

The RelChip™ RC2133209 is a 32Kx9 RAM (288K bit). It supports either full nine bit operation, or eight bit with parity operation for high reliability applications. Many interfaces can be used since the part separates the data input, data output, and address pins. Data input and output lines may be tied together with external directional control using the OE signal.

## Parity Configuration

The ninth data bit (on the DP/QP pin) is configured for data or parity by the PAR0 through PAR2 pins. These pins should all be tied high or low as required by the application. Table 1 shows the available configurations.

Table 1: Parity Selections

| PAR[2:0] | Parity Bit |
|---|---|
| 000 | Z |
| 001 | Data Bit 9 |
| 010 | Even Parity |
| 011 | Odd Parity |
| 1xx | Parity Error |

### Parity Mode 000

The DP/QP parity bit is not used. The user should tie the DP pin to GND if this mode is used.

### Parity Mode 001

The parity bit is a ninth data bit. Read/write operations are used.

### Parity Mode 010

The parity bit is an even parity bit. When data is written to the memory, the even parity of the eight data bits is calculated and stored in memory. When a read occurs, the even parity bit is output on the QP pin.

### Parity Mode 011

The parity bit is an odd parity bit. When data is written to the memory, the odd parity of the eight data bits is calculated and stored in memory. When a read occurs, the odd parity bit is output on the QP pin.

### Parity Mode 1xx

The parity bit is an error flag. When data is written to the memory, the parity of the eight data bits is calculated and stored in memory. When a read occurs, the stored bit is compared to the parity of the eight read bits. If there is a parity error, the QP pin is asserted (high). Otherwise, the QP pin remains low.

## Read

Read occurs when WEn is not asserted on the rising edge of the CLK (see Figure 2).

## Write

Write occurs when WEn is asserted on the rising edge of the CLK (see Figure 2).

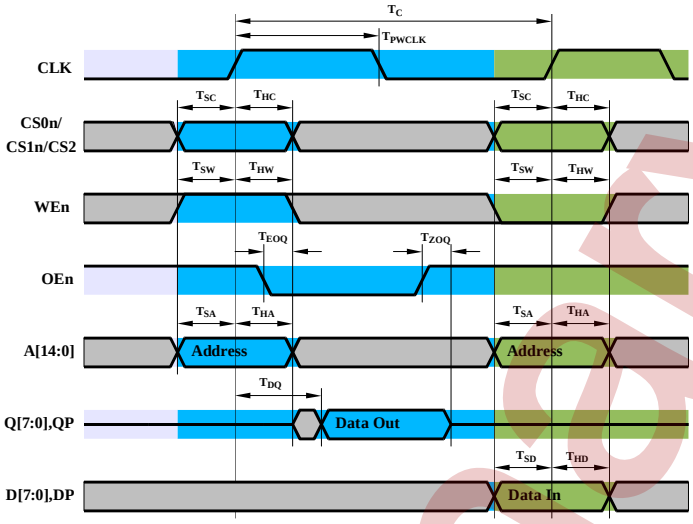



Figure 2: Waveforms

# SPECIFICATIONS

## Absolute Maximums (1)

Temperature ..... -55 to 350ºC
Power Supply ($V_{DD}$ referenced to ground) ..... -0.2 to 6.0 volts
Battery Voltage ($V_{DDB}$ referenced to ground) ..... -0.2 to 6.0 volts
IO Voltage (referenced to ground) ..... -0.2 to 6.0 volts

## Operating Conditions

Temperature (die temperature) ..... -55 to 300ºC
Power Supply ($V_{DD}$ referenced to ground) ..... 4.5 to 5.5 volts
Battery Voltage ($V_{DDB}$ referenced to ground) ..... 3.4 to ($V_{DD}$-0.1) volts
IO Voltage (referenced to ground) ..... 0.2 to ($V_{DD}$+0.2) volts

1. Exceeding the maximum specifications may cause permanent damage to the part

## DC Characteristics

Table 2: DC Characteristics

| Symbol | Description | Min | Typ | Max @225C | Max @300C | Unit | Note |
|---|---|---|---|---|---|---|---|
| T | Die Temperature | -55 | | 225 | 300 | ºC | |
| $V_{DD}$ | Digital Power Supply | 4.5 | 5 | 5.5 | 5.5 | V | |
| $V_{DDB}$ | Battery Power Supply | 3.4 | | $V_{DD}$-0.1 | $V_{DD}$-0.1 | V | 1 |
| $I_{DD}$ | Active Current | | | 2.5 | 3 | mA/MHz | 2 |
| $I_{DDS}$ | Standby Current (CS=deselect) | | | 1.5 | 2 | mA/MHz | 2,3 |
| $I_{DDB}$ | Battery Current ($V_{DD}$=0) | | | 0.005 | 8 | mA | 4 |
| $V_{OH}$ | Output High Voltage ($I_{OH}$=4mA) | 0.9*$V_{DD}$ | | | | V | |
| $V_{OL}$ | Output Low Voltage ($I_{OL}$=4mA) | | | 0.5 | | V | |
| $V_{IH}$ | Input High Voltage | 0.8*$V_{DD}$ | | | | V | |
| $V_{IL}$ | Input Low Voltage | | | 1.0 | | V | |
| $I_L$ | Input Current | | | 10 | | uA | |

Notes:

1. For systems not using battery backup, connect $V_{DDB}$ to GND.
2. No Output Load
3. All bus signals toggling simulating other memories on the bus.
4. When not running on the battery, this DC current must be added to active and standby currents.

## AC Characteristics

Table 3: AC Characteristics

| Symbol | Description | Min | Max @225C | Max @300C | Unit | Note |
|---|---|---|---|---|---|---|
| F | Frequency | | 10 | 8 | MHz | |
| $T_{PWCLK}$ | Pulse Width: CLK | 45 | | | nS | |
| $T_{DO}$ | Delay: Q from CLK ↑ | | 75 | 80 | nS | |
| $T_{EOO}$ | Enable: OEn ↓ to Q | TBD | TBD | TBD | nS | |
| $T_{ZOO}$ | Disable: OEn ↑ to Q | TBD | TBD | TBD | nS | |
| $T_{SA}$ | Setup: Address to CLK ↑ | TBD | | | nS | |
| $T_{SC}$ | Setup: CS to CLK ↑ | 65 | | | nS | |
| $T_{SD}$ | Setup: Data to CLK ↑ | TBD | | | nS | |
| $T_{SW}$ | Setup: WEn to CLK ↑ | 8 | | | nS | |
| $T_{HA}$ | Hold: Address from CLK ↑ | TBD | | | nS | |
| $T_{HC}$ | Hold: CS from CLK ↑ | 0 | | | nS | |
| $T_{HD}$ | Hold: Data from CLK ↑ | TBD | | | nS | |
| $T_{HW}$ | Hold: WEn from CLK ↑ | 0 | | | nS | |
| $T_{PWR}$ | Rise: $V_{DD}$ | 1 | | | mS | 1 |
| $T_{PWF}$ | Fall: $V_{DD}$ | 0 | | | nS | 1 |

Notes:

1. Sampled Only

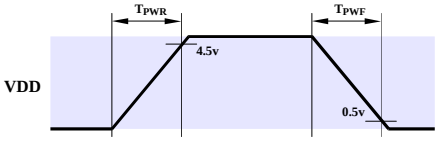



Figure 3: Power Supply Ramp

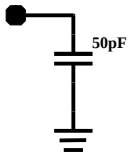



Figure 4: AC Measurement Load

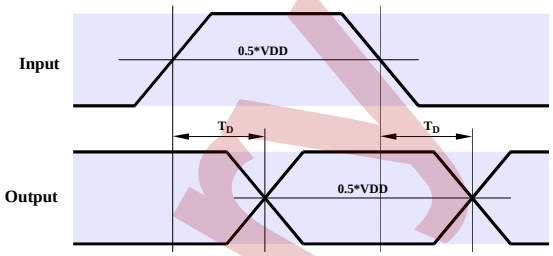



Figure 5: Delay Measurement

## PACKAGING

The RC2133209 is packaged in a 68 pin J-Lead QFP.

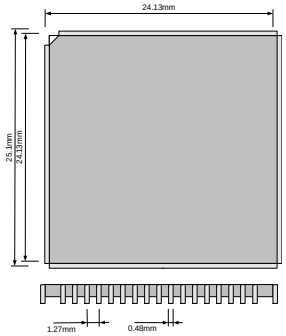



Table 4: Pin Out

| Pin | Name | Dir | Function | Pin | Name | Dir | Function |
|---|---|---|---|---|---|---|---|
| 1 | GND | Ground | Ground | 35 | GND | Ground | Ground |
| 2 | Q3 | TS | Data Output | 36 | A13 | Input | Address Input |
| 3 | D3 | Input | Data Input | 37 | A2 | Input | Address Input |
| 4 | Q5 | TS | Data Output | 38 | CS2 | Input | Chip Enable |
| 5 | D5 | Input | Data Input | 39 | nc | na | No Connection |
| 6 | Q7 | TS | Data Output | 40 | A4 | Input | Address Input |
| 7 | nc | na | No Connection | 41 | CLK | Input | Clock |
| 8 | D7 | Input | Data Input | 42 | A6 | Input | Address Input |
| 9 | VDD | Power | Power Supply | 43 | VDD | Power | Power Supply |
| 10 | GND | Ground | Ground | 44 | GND | Ground | Ground |
| 11 | CS0n | Input | Chip Enable (low active) | 45 | D6 | Input | Data Input |
| 12 | OEn | Input | Output Enable (low active) | 46 | Q6 | TS | Data Output |
| 13 | A7 | Input | Address Input | 47 | D4 | Input | Data Input |
| 14 | CS1n | Input | Chip Enable (low active) | 48 | Q4 | TS | Data Output |
| 15 | A5 | Input | Address Input | 49 | D2 | Input | Data Input |
| 16 | A14 | Input | Address Input | 50 | Q2 | TS | Data Output |
| 17 | VDD | Power | Power Supply | 51 | VDD | Power | Power Supply |
| 18 | GND | Ground | Ground | 52 | GND | Ground | Ground |
| 19 | A12 | Input | Address Input | 53 | WEn | Input | Write Select (low active) |
| 20 | A3 | Input | Address Input | 54 | nc | na | No Connection |
| 21 | A11 | Input | Address Input | 55 | PAR0 | Input | Parity Control Select |
| 22 | A1 | Input | Address Input | 56 | nc | na | No Connection |
| 23 | A10 | Input | Address Input | 57 | PAR1 | Input | Parity Control Select |
| 24 | A9 | Input | Address Input | 58 | VDDB | Power | Battery Backup Supply |
| 25 | A0 | Input | Address Input | 59 | nc | na | No Connection |
| 26 | VDD | Power | Power Supply | 60 | VDD | Power | Power Supply |
| 27 | GND | Ground | Ground | 61 | GND | Ground | Ground |
| 28 | nc | na | No Connection | 62 | DP | Input | Data 9 Input |
| 29 | A8 | Input | Address Input | 63 | QP | TS | Parity Output |
| 30 | nc | na | No Connection | 64 | D0 | Input | Data Input |
| 31 | PAR2 | Input | Parity Mode | 65 | Q0 | TS | Data Output |
| 32 | nc | na | No Connection | 66 | D1 | Input | Data Input |
| 33 | GND | Ground | Ground | 67 | Q1 | TS | Data Output |
| 34 | VDD | Power | Power Supply | 68 | VDD | Power | Power Supply |