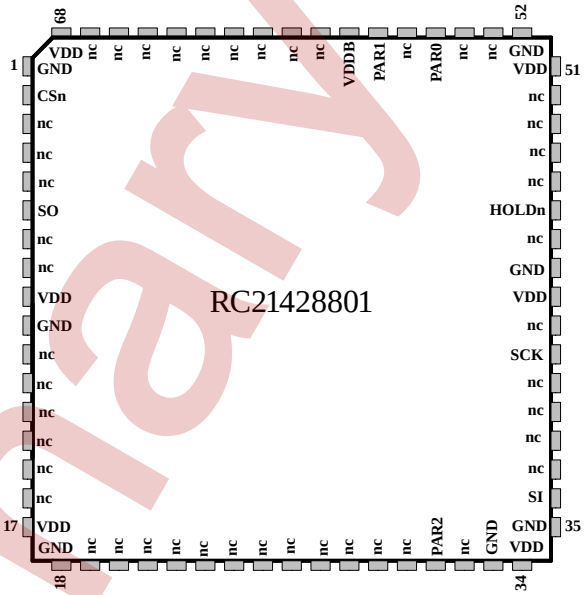
FEATURES

- 288K x 1 Serial Random Access Memory
- 8 MHz Clock
- 5 volt Power Supply
- 3.4 volt Battery Back Up
- Fully Static Design
- Wide Operating Temperature Range
- 32Kx9 Organization
- Multiple Operating Modes
  - Byte, 9-bit, or byte with parity
  - Single Byte
  - Page
  - Sequential
- 32x9 or 32x8 Page Operation



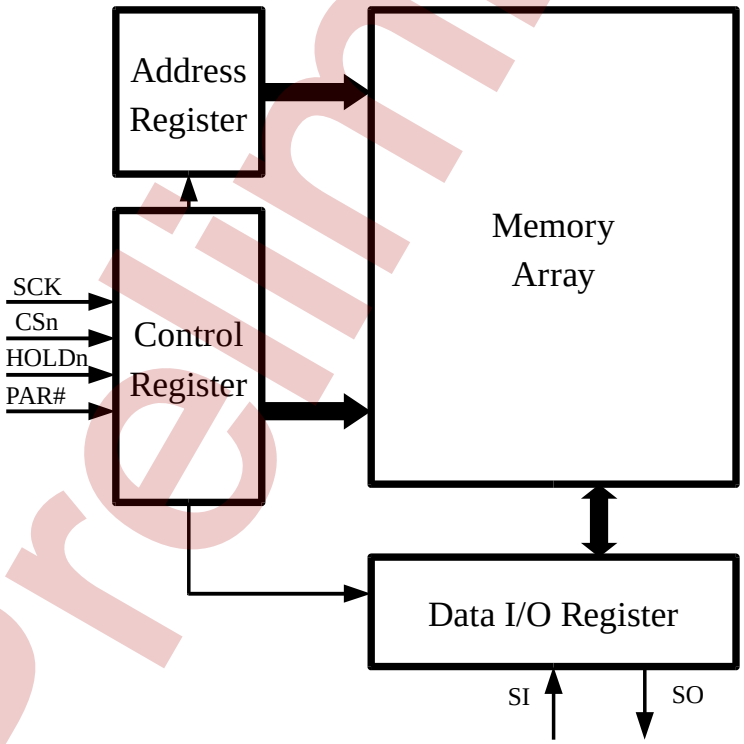


Figure 1: Block Diagram

General Description

The RelChip™ RC21428801 is a 288K by 1 bit serial RAM. The control, address, and data are transmitted to/from the memory via a SPI interface. The RC21428801 also provides parity options and programmable operating modes: byte, page, and sequential.

HOLDn is provided to interrupt operation during higher priority uses of the SPI interface. Once HOLDn is released, the RC21428801 will continue with the previous operation.

The RC21428801 includes battery backup to maintain memory state during power outages.

Modes of Operation

The RC21428801 can operate in byte, page, or sequential modes. In the byte mode, single bytes (or nine bits) are transferred on the serial peripheral interface (SPI) in response to an instruction. In page mode, 32 bytes (or nine bits) sections of the RAM are addressed. In the sequential mode, as many locations as desired can be used without reissue of the instruction.

Instructions

The RC21428801 responds to four instructions as shown in Table. These allow reading and writing of the memory, the configuration register, and the status register. The read and write commands are executed in the currently set mode.

Table 1: Instructions

Instruction	Instruction Code (b)	Description
Read	[0]00000011	Read according to the Mode
Write	[0]00000010	Write according to the Mode
ReadStatus	[0]00000101	Read the Status Register
WriteConfig	[0]00000001	Write the Configuration Register

Byte Operation

In the byte operation mode, single bytes (or nine bit words) are read and written as shown in Figure 2 through Figure 5. Figure 2 and Figure 4 show the byte operations while Figure 3 and Figure 5 show the nine bit operations. An instruction is clocked in first, followed by a 16-bit address (A15 is a “don’t care”). The part is then read or written. If CS is held low beyond the read or writing of the data, the same address is used for the next sequence. Writes do not occur until all eight (or nine) bits of data are transferred.

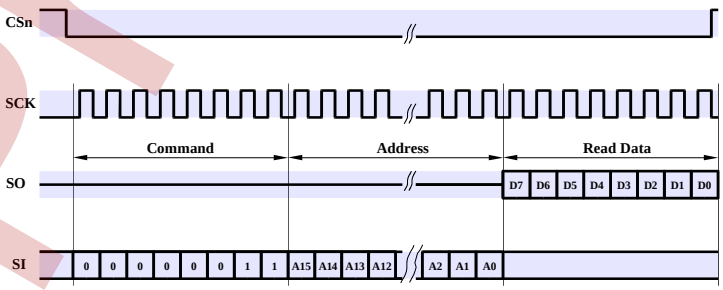


Figure 2: Byte Read Function

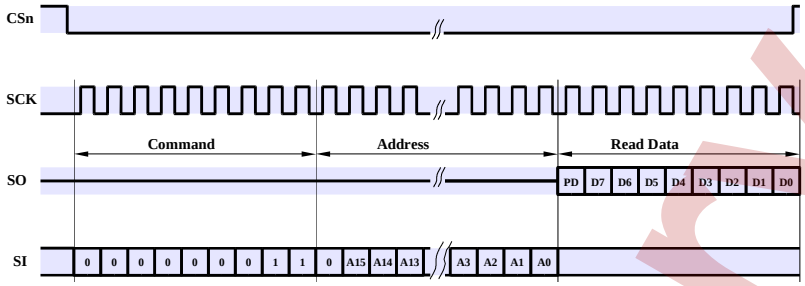


Figure 3: 9-Bit or Parity Byte Read Function

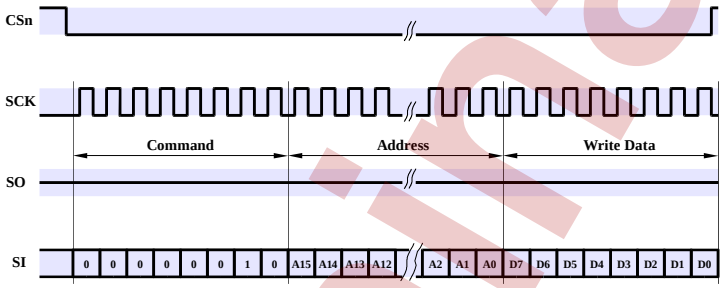


Figure 4: Byte Write Function

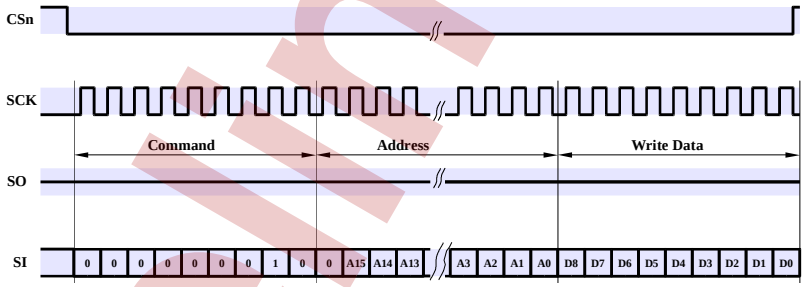


Figure 5: 9-Bit or Parity Byte Write Function

In the byte mode (PAR[2:0] == 000b), the instruction is eight bits as shown in Table 1. The table also shows the addition for the nine bit and parity modes (bit in []). In byte mode, an eight bit instruction is transmitted to the part, followed immediately by a sixteen bit address. A15 is not used. The data is then available, big Endean, on the next clock falling edge. Transmission (read or write) ends when CS is released (high).

In the nine bit data mode, the data field is extended one bit. For instructions, an extra “0” is prepended to the instruction, and the address field is constructed with appropriate extra “0”’s. Thus, the address field becomes the vector {0, A15, A14, A13, A12, A11, A10, A9, A8, 0, A7, A6, A5, A4, A3, A2, A1, A0}. The data vector is {D8, D7, D6, D5, D4, D3, D2, D1, D0} for all read and write operations.

The parity modes behave exactly like the nine bit data mode for instructions and addresses. However, D8 is ignored during a write (it still must be present). During a read, D8 becomes the parity output as described below.

Page Operation

The memory of the RC21428801 is segmented into 32 word (a word is eight bit or nine bit depending upon the mode) blocks addressed by A4 to A0. A page mode read or write will begin at exact byte address specified with the instruction. The address is increments with each operation on only the field A4 to A0 (modulo 32). Thus, page operations wrap within a page. Figure 6 and Figure 7 show the page write operation for eight bit words.

The page operation can be aborted (less than 32 words read) by releasing CS. Each page operation must be terminated by releasing CS (high).

The description of the eight bit and nine bit modes of byte operation is also valid for page operation. However, because of page wrapping, writes to more than 32 words will overwrite the data written on a first pass.

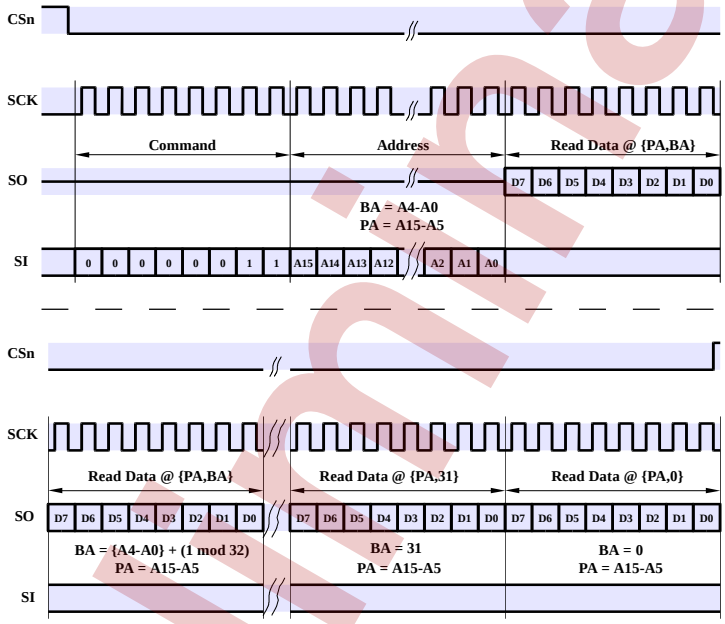


Figure 6: 8-Bit Page Read Function

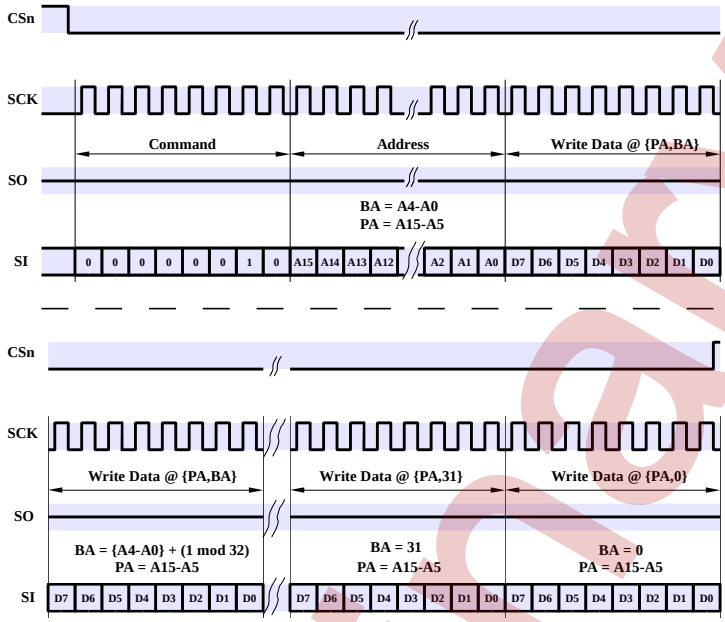


Figure 7: 8-Bit Page Write Function

Sequential Operation

An operation on the RC21428801 can be sequenced through any number of contiguous addresses in this mode. An operation begins by issuing the appropriate instruction (read or write), followed by the first address. The operation is then executed on sequential bytes until chip select (CSn) is deasserted. If the address counts from 0x7fff, it wraps to 0x0000. If more than 32K words are written, the value written the first time is overwritten on the second pass. Figure 8 and Figure 9 show the 8-bit word version of sequential read and write.

The description of the eight bit and nine bit modes of byte operation is also valid for page operation.

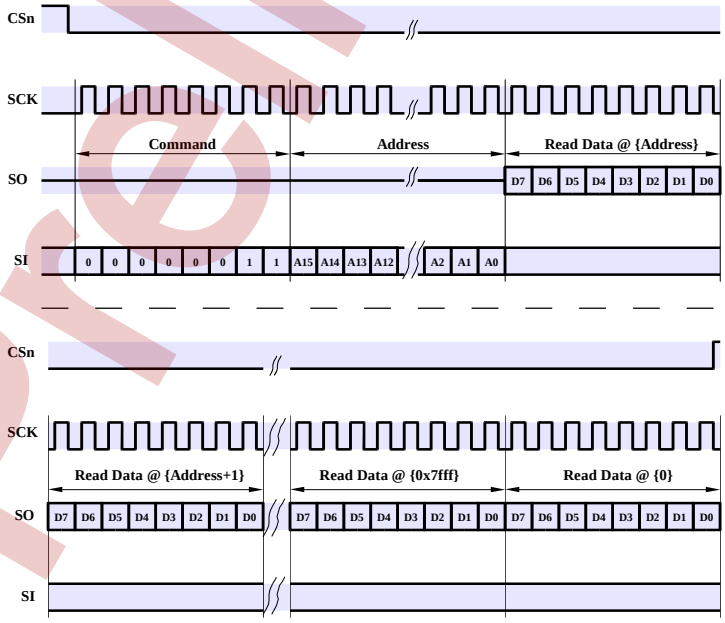


Figure 8: 8-Bit Sequential Read Function

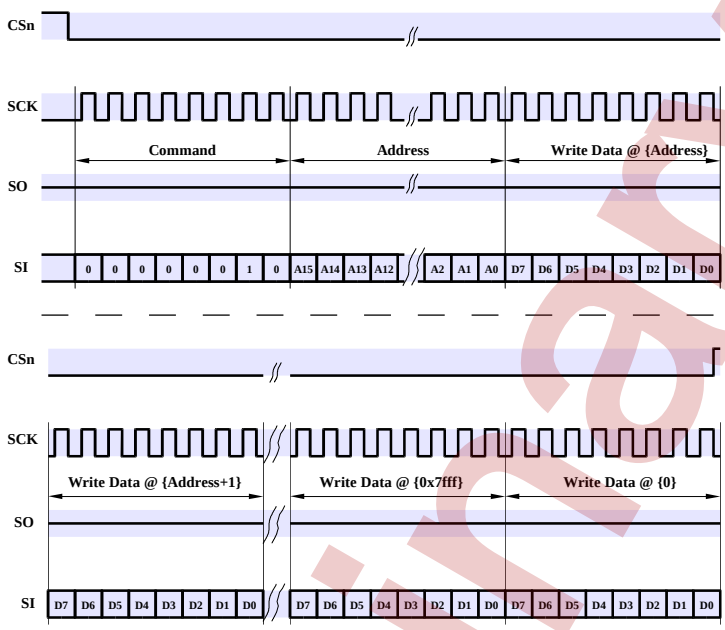


Figure 9: 8-Bit Sequential Write Function

HOLD Function

Error! Reference source not found. shows the hold function. When HOLDn is asserted (low), the current operation is suspended, but all state and data are maintained internally. When HOLDn is subsequently released (high), the RC21428801 resumes the operation at exactly the point it was when HOLDn was asserted. In applications that do not use the HOLD mode, HOLDn is tied to V_{DD}.

Configuration

The RC21428801 includes configuration for the read/write mode and a number of parity modes. These are set by writing the configuration register (see Table 2 and Table 3). The write status command sends exactly nine bits as indicated in Figure 10 and Figure 11.

Table 2: Configuration/Status Register

7	6	5	4	3	2	1	0
OM	OM	0	0	0	0	0	HOLD

Table 3: Operation Mode (OM)

7	6	Operation Mode	Default
0	0	Byte	X
0	1	Sequential	
1	0	Page	
1	1	DO NOT USE	

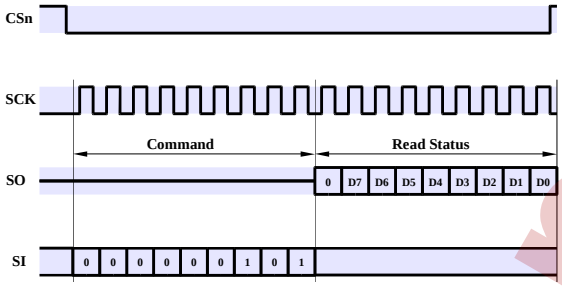


Figure 10: 9-Bit or Parity Status Read Function

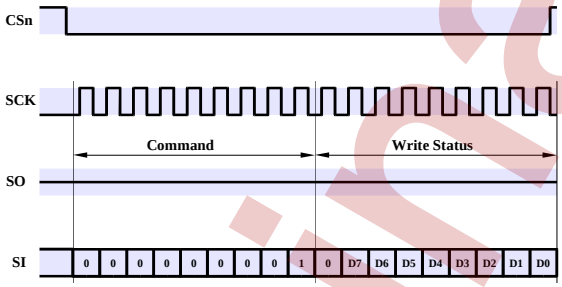


Figure 11: 9-Bit or Parity Configuration Write Function

Parity

Parity is set by connecting the PAR0 through PAR2 pins to power and ground. The options include eight bit data, nine bit data, eight bit with even parity, eight bit with odd parity, and eight bit with parity error as per Table 4.

Table 4: Parity Selections

PAR[2:0]	Parity Bit	default
000	Z	X
001	Data Bit 9	
010	Even Parity	
011	Odd Parity	
1xx	Parity Error	

8-Bit Data Words

The part operates with eight bit words throughout. No extra “0”s are inserted in the instruction and address fields.

9-Bit Data Words

The part operates with nine bit words throughout. Extra “0”s are inserted in the instruction and address fields as specified above. All data transfers are nine bit.

8-Bit with Even Parity Bit

The part operates as a nine bit word part on the interface. Extra “0”s are inserted in the instruction and address fields as specified above. During a write, the 9th bit is ignored. Internally, even parity for the eight bit portion of the word is calculated and stored. During a read, the stored even parity is read out as the 9th bit.

8-Bit with Odd Parity Bit

The part operates as a nine bit word part on the interface. Extra "0"s are inserted in the instruction and address fields as specified above. During a write, the 9th bit is ignored. Internally, odd parity for the eight bit portion of the word is calculated and stored. During a read, the stored odd parity is read out as the 9th bit.

8-Bit Plus Parity Error Flag

The part operates as a nine bit word part on the interface. Extra "0"s are inserted in the instruction and address fields as specified above. During a write, the 9th bit is ignored. Internally, parity for the eight bit portion of the word is calculated and stored. During a read, the stored parity is compared to a new parity calculation on the stored parity. Any difference is reported as a "1" on the 9th bit. No parity error is reported as a "0".

Exceptions

The RC21428801 handles exceptions as required. These conditions are early termination of an operation, termination of an operation during the word transmission, detection of parity errors, invalid instruction, and invalid status register mode.

Early Termination of an Operation

The page mode implies 32 words will be read or written. However, early termination of the page mode operation (releasing CS, high, before 32 words are transferred) causes no problems. For example in page mode, one could release CS after ten words, transferring only those ten. The next instruction will be read when CS is asserted again.

Termination of an Operation during Word Transmission

If CS is released in the middle of a word transmission, no negative effects will occur. The part will not write a word until all bits of the word are received. Since they are not yet received, the part ignores what is has received.

Detection of Parity Errors

Parity errors are reported by the RC21428801. These can either be reported as the actual parity bit or parity error flag. The part considers this as combinatorial results, with no internal action required. The part remains ready of the next operation.

Invalid Instruction

If an instruction other than the ones of Table 1 is used, the RC21428801 treats it as a NOP. The part will not respond until after CS has been released.

Invalid Status Register Mode

The valid status register modes are "00", "01', and "10". If one attempts to write "11" into the register, the part will ignore the operation. The previous contents of the status register are maintained.

SPI Interface

To do any operation, the part communicates on a serial peripheral interface (SPI) interface. The following figures show the timing relationship for communication.

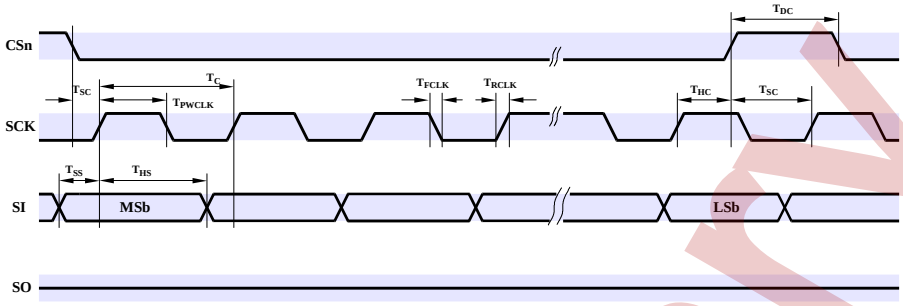


Figure 12: Serial Input Timing

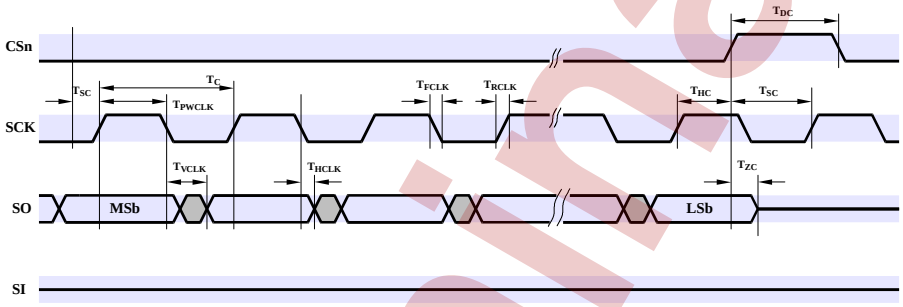


Figure 13: Serial Output Timing

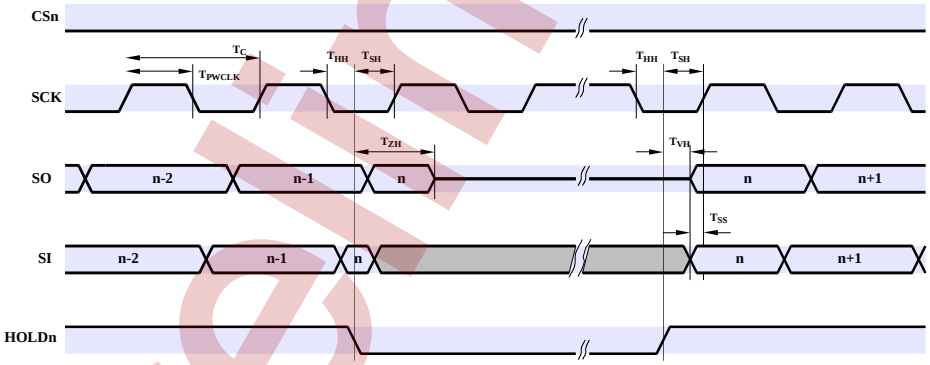


Figure 14: Hold Timing

SPECIFICATIONS

Absolute Maximums (1)

Temperature ..... -55 to 350ºC
Power Supply (V_{DD} referenced to ground) ..... -0.3 to 6.0 volts
Battery Voltage (V_{DDB} referenced to ground) ..... -0.3 to 6.0 volts
IO Voltage (referenced to ground) ..... -0.3 to 6.0 volts

Operating Conditions

Temperature (die temperature) ..... -55 to 300ºC
Power Supply (V_{DD} referenced to ground) ..... 4.5 to 5.5 volts
Battery Voltage (V_{DDB} referenced to ground) ..... 3.4 to (V_{DD}-0.1) volts
IO Voltage (referenced to ground) ..... -0.2 to (V_{DD}+0.2) volts

1. Exceeding the maximum specifications may cause permanent damage to the part

DC Characteristics

Table 5: DC Characteristics

Symbol	Description	Min	Typ	Max @225C	Max @300C	Unit	Note
T	Temperature	-55	25	225	300	ºC	
V_{DD}	Digital Power Supply	4.5	5	5.5	5.5	V	
V_{DDB}	Battery Power Supply	3.4		V_{DD}-0.1	V_{DD}-0.1	V	1
I_{DD}	Active Current			0.25	0.5	mA/MHz	2,3
I_{DDS}	Standby Current (CSn=1)			0.5	2.5	mA/MHz	2,3
I_{DDB}	Battery Current (V_{DD}=0)			0.005	8	mA	
V_{OH}	Digital Output High Voltage (I_{OH}=2mA)	0.9*V_{DD}				V	
V_{OL}	Digital Output Low Voltage (I_{OL}=2mA)			0.5	0.5	V	
V_{IH}	Digital Input High Voltage	0.8*V_{DD}				V	
V_{IL}	Digital Input Low Voltage			1.0	1.0	V	
I_L	Digital Input Current			10	10	uA	

Notes:

1. For systems not using battery backup, connect V_{DDB} to GND.
2. No Output Load
3. Calculated as I(10MHz)/10

AC Characteristics

Table 6: AC Characteristics

Symbol	Description	Min	Max @225C	Max @300C	Unit	Note
F	Frequency		10	8	MHz	
T_{PWCLK}	Pulse Width: CLK	45		55	nS	
T_{VCLK}	Delay: SCK ↓ to SO		TBD	TBD	nS	
T_{VH}	Delay: HOLDn ↑ to SO		TBD	TBD	nS	
T_{DC}	Disable Width: CSn	TBD			nS	
T_{HCLK}	Hold Time: SO from SCK ↓	0			nS	
T_{ZC}	Disable: SO from CSn ↓	TBD	TBD	TBD	nS	
T_{ZH}	Disable: SO from HOLDn ↓	TBD	TBD	TBD	nS	
T_{SC}	Setup: CSn ↓ from SCK ↑	TBD	TBD	TBD	nS	
T_{SH}	Setup: HOLDn to SCK ↑	TBD	TBD	TBD	nS	
T_{SS}	Setup: SI to CLK ↑	TBD	TBD	TBD	nS	
T_{HC}	Hold: CSn ↑ to SCK ↑	TBD	TBD	TBD	nS	
T_{HH}	Hold: HOLDn from SCK ↑	TBD	TBD	TBD	nS	
T_{HS}	Hold: SI from CLK ↑	TBD	TBD	TBD	nS	

PACKAGING

The RC21428801 is packaged as a 68 pin J-Lead QFP.

Table 7: Pin Out

Pin	Name	Dir	Function	Pin	Name	Dir	Function
1	GND	Ground	Ground	35	GND	Ground	Ground
2	CSn	Input	Chip Select (Low Active)	36	SI	Input	Data Input
3	nc	na	No Connection	37	nc	na	No Connection
4	nc	na	No Connection	38	nc	na	No Connection
5	nc	na	No Connection	39	nc	na	No Connection
6	SO	TS	Data Output	40	nc	na	No Connection
7	nc	na	No Connection	41	SCLK	Input	Clock
8	nc	na	No Connection	42	nc	na	No Connection
9	VDD	Power	Power Supply	43	VDD	Power	Power Supply
10	GND	Ground	Ground	44	GND	Ground	Ground
11	nc	na	No Connection	45	nc	na	No Connection
12	nc	na	No Connection	46	HOLDn	Input	Hold Control (Low Active)
13	nc	na	No Connection	47	nc	na	No Connection
14	nc	na	No Connection	48	nc	na	No Connection
15	nc	na	No Connection	49	nc	na	No Connection
16	nc	na	No Connection	50	nc	na	No Connection
17	VDD	Power	Power Supply	51	nc	na	No Connection
18	GND	Ground	Ground	52	nc	na	No Connection
19	nc	na	No Connection	53	nc	na	No Connection
20	nc	na	No Connection	54	nc	na	No Connection
21	nc	na	No Connection	55	PAR0	Input	Parity Control
22	nc	na	No Connection	56	nc	na	No Connection
23	nc	na	No Connection	57	PAR1	Input	Parity Control
24	nc	na	No Connection	58	VDDB	Power	Battery Backup Supply
25	nc	na	No Connection	59	nc	na	No Connection
26	nc	na	No Connection	60	nc	na	No Connection
27	nc	na	No Connection	61	nc	na	No Connection
28	nc	na	No Connection	62	nc	na	No Connection
29	nc	na	No Connection	63	nc	na	No Connection
30	nc	na	No Connection	64	nc	na	No Connection
31	PAR2	Input	Parity Control	65	nc	na	No Connection
32	nc	na	No Connection	66	nc	na	No Connection
33	GND	Ground	Ground	67	nc	na	No Connection
34	VDD	Power	Power Supply	68	VDD	Power	Power Supply