FEATURES

- **-55°C to 300°C Temperature Range**
- ARM® 32-bit Cortex®-M0 Core
  - ARMv6-M Thumb®-2 Instruction Set
  - Thirty-two bit Single-Cycle Multiplier
  - Serial Wire Debug
  - Nested Vectored Interrupt Controller (NVIC)
  - Interrupts: Twenty-one Peripheral and Six System
  - Watchdog Timer
  - Breakpoints
  - System Tick Timer
- Memory
  - 4K Byte Internal SRAM
  - Internal Boot ROM
  - Expansion Bus
- Single 5 volt supply
- SSP
  - SPI, SSP, Microwire
  - RX and TX FIFOs
  - Master or Slave
- UART
  - RS232 and RS485
  - RX and TX FIFOs
  - 16550 Compatible
  - LIN 2.0 Interface
- Programmable Watchdog Timer (WDT)
- Clock Options
  - Crystal Oscillator
  - Clock Output
  - Programmable Peripheral Clock Domains
- Timer/Counters
  - Two16 Bit
  - Two 32 Bit
  - PWM Outputs
  - NOS Outputs
- Real-time Counter
- Power management
  - Power on Reset (POR)
  - Reduced Power Modes: Sleep and Deep-Sleep.

GENERAL DESCRIPTION

The RelChip® RC10001 32-bit microcontroller is a full featured processor core and peripherals. It is designed in a high-temperature SOI process to operate from -55ºC to 300ºC reliably. The part operates up to 4MHz.

The ARM Cortex-M0 is the core processor. The ARM core contains a system tick timer, a watchdog timer, a nested vector interrupt controller (NVIC), register banks, and memory. Power control and sleep modes reduce the power consumption. The Cortex-M0 uses the advanced Thumb-2 instruction set.

Peripherals include a UART interface, a SPI interface, a LIN interface, four timer/counters with one capture input and four match outputs, a real-time counter, and up to ninety general purpose input/output (GPIO) pins.

The RC10001 32-bit ARM Cortex-M0 microcontroller is designed for extreme environment applications such as down-hole oil, gas, and geothermal applications, automotive, aerospace, industrial control, and utilities.

This document is a description of the product capability. Please refer to the *RC10001 User Manual* for a complete memory, peripheral, and register description.

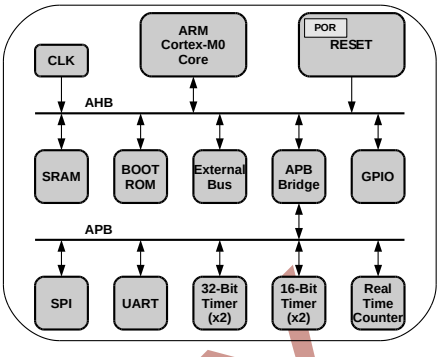

Figure 1: Block Diagram

ARM CORTEX-M0 CORE

The ARM core is a 32-bit machine utilizing the 16-bit Thumb-2 instruction set. All control registers and periphery are memory-mapped. This efficient, yet simple core achieves a performance of 0.45DMIPS/MHz on the Dhrystone benchmark.[1] A complete description of the ARM Cortex-M0 can be found in the *ARMv6-M Architecture Reference Manual* and the *Cortex-M0 Technical Reference Manual*.

The RC10001 configuration of the core includes single cycle thirty-two bit multiply, thread and handler modes of processor execution (including two stacks), twenty-seven interrupts (6 system plus 21 peripheral, programmable priority), three sleep modes, serial wire debug, and uses both AHB and APB ARM Buses internally.

The M0 core includes general purpose registers (twelve), special purpose registers (four), and dual stack pointers. Operation in either thread or handler mode is supported.

Clock

The clock can be driven by either a crystal between XTAL1 and XTAL2, or a CMOS input to XTAL1 (Figure 2). The RC10001 operates from DC to 4MHz. The clock input can be divided by up to 255 to save power. The program can dynamically change this divisor. The system clock, or the divided XTAL1 clock, can be further divided and output on the CLKOUT pin to synchronize systems.

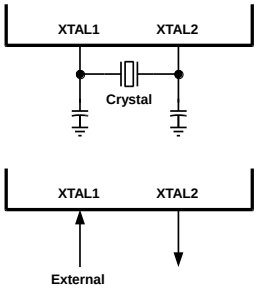

Figure 2: Clock Options

Nested Vector Interrupt Control (NVIC)

Twenty-seven interrupt sources are provided: six system and twenty-one peripheral (see Table 1) interrupts. Each peripheral may have multiple interrupt sources further expanding the interrupt span. Interrupt priority is programmable for all peripheral interrupts. All except reset, non-maskable, and hard fault interrupts are enabled and disabled under program control.

[1] http://www.arm.com/products/processors/cortex-m/cortex-m0.php

Table 1: Interrupts

Interrupt	Priority	Description
1=Reset	-2	Reset
2=NMI	-1	Non-Maskable
3=HardFault	0	Faults
11=SVCall	0	Service Call
14=PendSV	0	Pending Service Call
15=SysTick	0	System Tick
16=Wakeup	Program (1)	Wake Up Pin
17=RAM	Program	RAM
18=T16A	Program	Timer/Counter, 16-Bit
19=T16B	Program	Timer/Counter, 16-Bit
20=T32A	Program	Timer/Counter, 32-Bit
21=T32B	Program	Timer/Counter, 32-Bit
22=SSP	Program	SPI Port
23=UART	Program	UART Port
24=WDT	Program	Watchdog Timer
25=SVC1	Program	Service Call
26=GPIO0	Program	General Purpose IO, Port 0
27=GPIO1	Program	General Purpose IO, Port 1
28=GPIO2	Program	General Purpose IO, Port 2
29=GPIO3	Program	General Purpose IO, Port 3
30=GPIO4	Program	General Purpose IO, Port 4
31=GPIO5	Program	General Purpose IO, Port 5
32=GPIO6	Program	General Purpose IO, Port 6
33=GPIO7	Program	General Purpose IO, Port 7
34=RTC	Program	Real Time Clock
35=SVC2	Program	Service Call
36=EXBUS	Program	External Bus

Notes:

1. Wakeup interrupts can be programmed from multiple sources, including external pins.

Reset Options

Soft and hard reset entries to the processor are provided. A hard reset will load the boot code before beginning program execution. Four sources for the boot code are available.

Soft reset occurs whenever code is already boot loaded and has not been disturbed. A battery backup voltage decreases the probability of boot code reloading.

The program code must be loaded immediately following a hard reset. This code can come from one of four sources: the serial wire debug port, the UART port, the SSP port, or external memory.

Sleep Modes

Three sleep modes are used to reduce power. Basic sleep mode disables the clock to the core and memory. Deep sleep mode adds disabling the clock to most peripherals. Deep power-down mode also disables the watchdog timer.

In basic sleep mode, an interrupt generated by any peripheral will “wake up” the microcontroller. In deep sleep mode, the WAKEUP pin and the watchdog timer can “wake up” the microcontroller. The individual peripheral clocks are disabled to reduce power in deep sleep.

System Tick Timer Peripheral

The system tick timer is a programmable twenty-four bit down counter. An interrupt, if enabled, is generated. “Time slices” for code can be generated for multithread software, or time synchronization.

MEMORY

The RC10001 contains an internal 4KByte of SRAM for program and data storage. It also contains a boot ROM, not normally accessed by the user. For larger systems, the RC10001 contains a full thirty-two bit, address/data multiplexed external bus. The external bus can address up to 2GByte of external memory.

Memory parity is checked on a per byte basis. Parity error interrupt enables for internal SRAM, internal ROM, and external memory are set by the programmer. Battery backup power is provided for the internal RAM.

All peripherals are memory mapped as shown in Figure 4.

PERIPHERALS

The RC10001 peripherals are designed to maximize product applications. Ninety pins serve dual functions: a built in peripheral function (such as UART, SPI, etc.), or General Purpose Input/Output (GPIO). Function or GPIO is configured for each pin individually. Thus, a system can include a SPI, an UART, four timer/counters, and an external bus, or configure some or all of these pins for GPIO.

All pins are configured as GPIO pins with an internal pull-up connected at reset. They then can be configured as shown in Figure 3 for either the function or GPIO and with or without internal pull up or down devices.

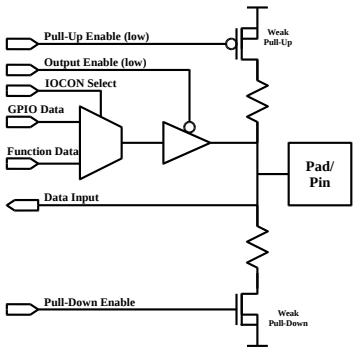

Figure 3: IO Configuration

General Purpose IO (GPIO)

Ninety of the pins on the RC10001 can be set for GPIO or configured to a function (see Table 2). Each individual pin (as opposed to the whole port) can be configured as GPIO or as a participant in the function. The input signal is routed to both the function and the GPIO register. The GPIO registers are mask written, avoiding glitches.

GPIO pins can also be interrupt inputs for either level or edge sensitive interrupts. Either polarity, rising edge, falling edge, or both edges can be selected.

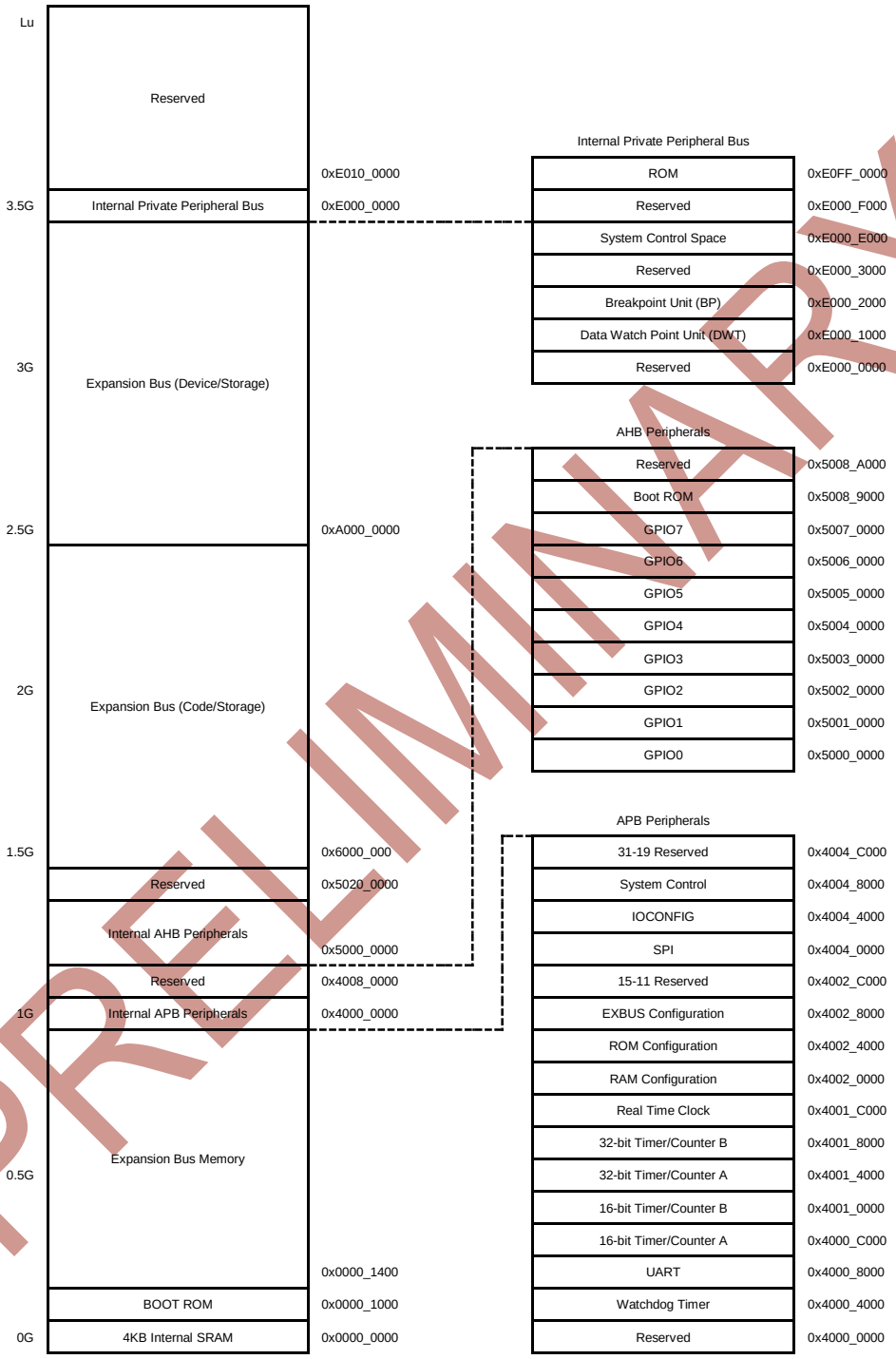

Figure 4: Memory Map

Table 2: GPIO/Function Pin Selection

Pin	GPIO	Function	Pin	GPIO	Function
SCLK_GPIO0_0	GPIO0[0]	SPI Clock	EBW0n_GPIO3_9	GPIO3[9]	External Bus Byte Write 0
MISO_GPIO0_1	GPIO0[1]	SPI Master Input	EBW1n_GPIO3_10	GPIO3[10]	External Bus Byte Write 1
MOSI_GPIO0_2	GPIO0[2]	SPI Master Output	EBW2n_GPIO3_11	GPIO3[11]	External Bus Byte Write 2
SSELA_GPIO0_3	GPIO0[3]	SPI Select A	EBW3n_GPIO4_0	GPIO4[0]	External Bus Byte Write 3
SSELB_GPIO0_4	GPIO0[4]	SPI Select B	EWAIT_GPIO4_1	GPIO4[1]	External Bus Wait
SSELC_GPIO0_5	GPIO0[5]	SPI Select C	ECRE_GPIO4_2	GPIO4[2]	External Bus Configuration Enable
SSELD_GPIO0_6	GPIO0[6]	SPI Select D	EINT_GPIO4_3	GPIO4[3]	External Bus Interrupt
T16ACAP0_GPIO0_7	GPIO0[7]	Timer 16A Capture	EADQ0_GPIO4_4	GPIO4[4]	External Bus A/D 0
T16AMAT0_GPIO0_8	GPIO0[8]	Timer 16A Match 0	EADQ1_GPIO4_5	GPIO4[5]	External Bus A/D 1
T16AMAT1_GPIO0_9	GPIO0[9]	Timer 16A Match 1	EADQ2_GPIO4_6	GPIO4[6]	External Bus A/D 2
T16AMAT2_GPIO0_10	GPIO0[10]	Timer 16A Match 2	EADQ3_GPIO4_7	GPIO4[7]	External Bus A/D 3
T16AMAT3_GPIO0_11	GPIO0[11]	Timer 16A Match 3	EADQ4_GPIO4_8	GPIO4[8]	External Bus A/D 4
T16BCAP0_GPIO1_0	GPIO1[0]	Timer 16B Capture	EADQ5_GPIO4_9	GPIO4[9]	External Bus A/D 5
T16BMAT0_GPIO1_1	GPIO1[1]	Timer 16B Match 0	EADQ6_GPIO4_10	GPIO4[10]	External Bus A/D 6
T16BMAT1_GPIO1_2	GPIO1[2]	Timer 16B Match 1	EADQ7_GPIO4_11	GPIO4[11]	External Bus A/D 7
T16BMAT2_GPIO1_3	GPIO1[3]	Timer 16B Match 2	EADQ8_GPIO5_0	GPIO5[0]	External Bus A/D 8
T16BMAT3_GPIO1_4	GPIO1[4]	Timer 16B Match 3	EADQ9_GPIO5_1	GPIO5[1]	External Bus A/D 9
T32ACAP0_GPIO1_5	GPIO1[5]	Timer 32A Capture	EADQ10_GPIO5_2	GPIO5[2]	External Bus A/D 10
T32AMAT0_GPIO1_6	GPIO1[6]	Timer 32A Match 0	EADQ11_GPIO5_3	GPIO5[3]	External Bus A/D 11
T32AMAT1_GPIO1_7	GPIO1[7]	Timer 32A Match 1	EADQ12_GPIO5_4	GPIO5[4]	External Bus A/D 12
T32AMAT2_GPIO1_8	GPIO1[8]	Timer 32A Match 2	EADQ13_GPIO5_5	GPIO5[5]	External Bus A/D 13
T32AMAT3_GPIO1_9	GPIO1[9]	Timer 32A Match 3	EADQ14_GPIO5_6	GPIO5[6]	External Bus A/D 14
T32BCAP0_GPIO1_10	GPIO1[10]	Timer 32B Capture	EADQ15_GPIO5_7	GPIO5[7]	External Bus A/D 15
T32BMAT0_GPIO1_11	GPIO1[11]	Timer 32B Match 0	EADQ16_GPIO5_8	GPIO5[8]	External Bus A/D 16
T32BMAT1_GPIO2_0	GPIO2[0]	Timer 32B Match 1	EADQ17_GPIO5_9	GPIO5[9]	External Bus A/D 17
T32BMAT2_GPIO2_1	GPIO2[1]	Timer 32B Match 2	EADQ18_GPIO5_10	GPIO5[10]	External Bus A/D 18
T32BMAT3_GPIO2_2	GPIO2[2]	Timer 32B Match 3	EADQ19_GPIO5_11	GPIO5[11]	External Bus A/D 19
RxD_GPIO2_3	GPIO2[3]	UART Receive Data	EADQ20_GPIO6_0	GPIO6[0]	External Bus A/D 20
TxD_GPIO2_4	GPIO2[4]	UART Transmit Data	EADQ21_GPIO6_1	GPIO6[1]	External Bus A/D 21
CTSn_GPIO2_5	GPIO2[5]	UART Clear-to-Send	EADQ22_GPIO6_2	GPIO6[2]	External Bus A/D 22
DSRn_GPIO2_6	GPIO2[6]	UART Data Ready	EADQ23_GPIO6_3	GPIO6[3]	External Bus A/D 23
RIn_GPIO2_7	GPIO2[7]	UART Ring	EADQ24_GPIO6_4	GPIO6[4]	External Bus A/D 24
DCDn_GPIO2_8	GPIO2[8]	UART Carrier Detect	EADQ25_GPIO6_5	GPIO6[5]	External Bus A/D 25
RTSn_GPIO2_9	GPIO2[9]	UART Request-to-Send	EADQ26_GPIO6_6	GPIO6[6]	External Bus A/D 26
DTRn_GPIO2_10	GPIO2[10]	UART Terminal Ready	EADQ27_GPIO6_7	GPIO6[7]	External Bus A/D 27
OUT1_GPIO2_11	GPIO2[11]	UART Output 1	EADQ28_GPIO6_8	GPIO6[8]	External Bus A/D 28
OUT2_GPIO3_0	GPIO3[0]	UART Output 2	EADQ29_GPIO6_9	GPIO6[9]	External Bus A/D 29
ECLK_GPIO3_1	GPIO3[1]	External Bus Clock	EADQ30_GPIO6_10	GPIO6[10]	External Bus A/D 30
EACSAn_GPIO3_2	GPIO3[2]	External Bus Chip Select A	EADQ31_GPIO6_11	GPIO6[11]	External Bus A/D 31
EACSBn_GPIO3_3	GPIO3[3]	External Bus Chip Select B	EPDQ0_GPIO7_0	GPIO7[0]	External Bus Parity 0
EACSCn_GPIO3_4	GPIO3[4]	External Bus Chip Select C	EPDQ1_GPIO7_1	GPIO7[1]	External Bus Parity 1
EACSDn_GPIO3_5	GPIO3[5]	External Bus Chip Select D	EPDQ2_GPIO7_2	GPIO7[2]	External Bus Parity 2
EADVn_GPIO3_6	GPIO3[6]	External Bus Address Strobe	EPDQ3_GPIO7_3	GPIO7[3]	External Bus Parity 3
EWEn_GPIO3_7	GPIO3[7]	External Bus Write Enable	SWCLK_GPIO7_4	GPIO7[4]	Serial Debug Clock
EOEn_GPIO3_8	GPIO3[8]	External Bus Output Enable	SWDIO_GPIO7_5	GPIO7[5]	Serial Debug Data

Universal Asynchronous Receiver/Transmitter (UART)

The UART is a 16550-compatible peripheral. It supports both RS232 and RS485 protocols as well as LIN 2.0. The UART includes:

- Programmable baud rate generator: DC to 460Kbaud (with 3.6864MHz crystal)
- Protocols
  - RS232
  - RS485
  - LIN 2.0
- Separate RX and TX FIFOs: sixteen bytes deep, interrupt trigger at 1, 4, 8, or 16 bytes.
- Communication bits: Start, 1 or 2 Stop, and Even/Odd/Sticky/No Parity
- 5, 6, 7, or 8-bit data
- False start bit detection
- Line break generation and detection
- Independent interrupt masking
  - Receiver Status
  - Receive FIFO Trigger Level or Receiver Timeout
  - Transmit FIFO Empty
  - Modem Status
- Modem control functions: CTS, RTS, DSR, DTR, DCD, RI, OUT1, OUT2

Local Interconnect Network (LIN)

The UART and one of the thirty-two bit timers are used to implement the LIN 2.0 interface.

When receiving data, the hardware detects a Sync Break followed by a Sync Data field. The Sync Data field is used to auto detect the baud rate. Data is then received through the UART receive FIFO.

When transmitting data, the hardware sends the Sync Break (programmable from 13 to 16 bit times), followed by the UART transmit data FIFO contents.

Synchronous Serial Port (SSP)

The Synchronous Serial Port, also called the Serial Peripheral Interface (SPI), is a configurable serial interface. This serial interface can be configured as a Motorola Serial Peripheral Interface (SPI™), a 4-wire synchronous serial port (SSP), or a National Semiconductor Microwire™ bus. The part can be configured as the master, or as the slave, serial connection. The port features include:

- Master or slave node
- Full-duplex four wire transmission
- Data rate: DC to 1Mbps
- Programmable clock polarity and phase
- Transmit and receive FIFOs: eight deep, sixteen wide
- Data four to sixteen bits wide
- Programmable frame format: SPI, SSI, or Microwire
- Programmable Interrupts:
  - Transmit FIFO Empty
  - Receive FIFO
  - Receive FIFO Overrun
  - Receive data after idle period
- Loopback test mode

Timer/Counters

The RC10001 contains 4 timer/counters, two 16- bit and two 32-bit. Each timer/counter has an internal pre-scalar, four match registers (and outputs), a capture input, a PWM mode, and a NOS (non-overlapping signal) mode.

Table 3: Timer/Counter Pins

Generic	Timer 16A	Timer 16B	Timer 32A	Timer 32B
Capture	T16ACAP0	T16BCAP0	T32ACAP0	T32BCAP0
Match 0	T16AMAT0	T16BMAT0	T32AMAT0	T32BMAT0
Match 1	T16AMAT1	T16BMAT1	T32AMAT1	T32BMAT1
Match 2	T16AMAT2	T16BMAT2	T32AMAT2	T32BMAT2
Match 3	T16AMAT3	T16BMAT3	T32AMAT3	T32BMAT3

The two 16-bit counter registers have corresponding 16-bit pre-scalars while the 32-bit counter registers have 32-bit pre-scalars. The counter register can be reset by a match register (programmable) or a capture. Each match register can be programmed to be in normal, pulse width modulated (PWM), or non-overlapping signal (NOS) mode. The capture input can be used as the clock input for the counter register, of the internal clock can be used.

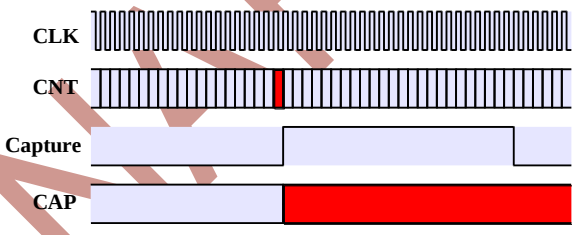

Figure 5: Timer/Counter Capture

Capture

The capture input is used as trigger input. Events on the capture pins cause the value from the counter register (CNT) to be written into the capture register (CAP). Possible events are a rising edge, a falling edge, or either edge. This write can, if enabled, generate an interrupt. A capture of a rising event is shown in Figure 5. The count and capture valid value is shown in red.

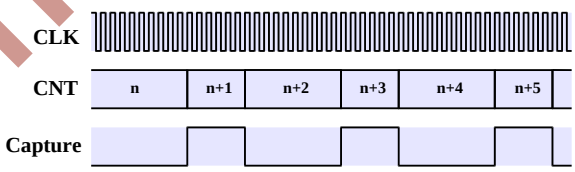

Figure 6: Timer/Counter Count

Counter

The capture input can be the clock input to the counter register (CNT). Thus, the capture pin events will be counted. These events can be rising edges, falling edges, or both edges. An example of counting on both edges is shown in Figure 6.

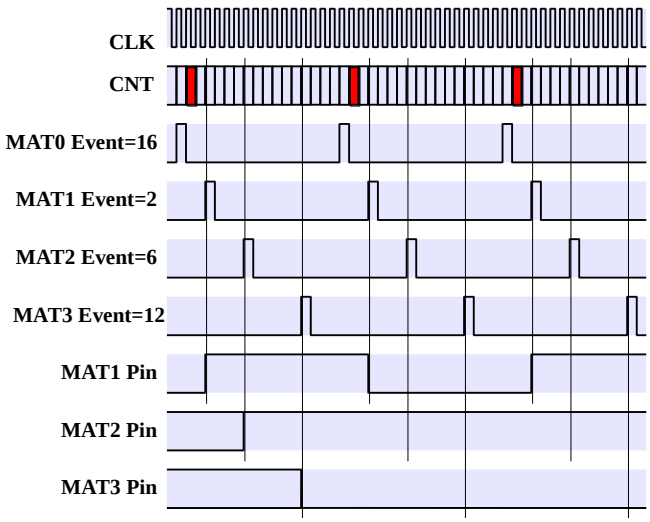

Figure 7: Timer/Counter Match

Timer Match (normal)

The match registers (MAT0 to MAT3) generate a match event whenever the value of the match register equals the value of the counter register. The event causes one or more actions based upon the configuration programmed. The event can reset the counter, stop the counter, generate a signal on the associated match output pin, and/or generate an interrupt.

Possible events on the match output pins are set high, set low, or toggle. The match output can be inverted. The example shown in Figure 7 illustrates this. In the example, match 0 is programmed to reset the counter at count 16. Match 1 is programmed to match at count 2, and invert the match 1 output pin. Match 2 is programmed to match at count 6, and set the match 2 output pin high. Match 3 is programmed to match at count 12, and set the match 3 output pin low.

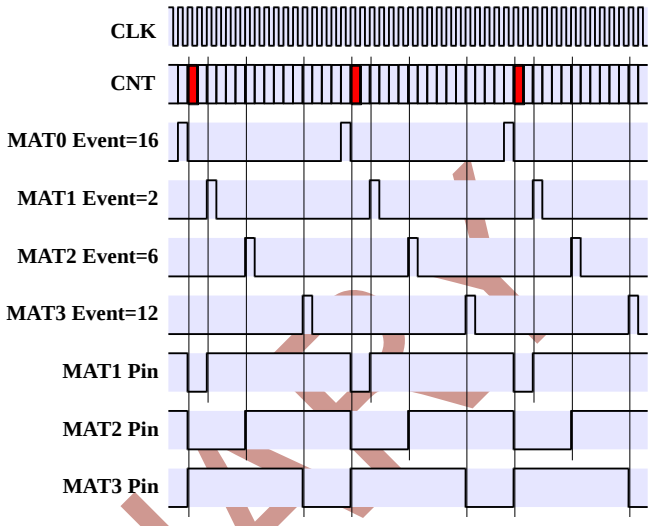

Figure 8: Timer/Counter PWM

PWM Mode

In PWM mode, one of the match registers (MAT0-3) is used as a reset for the counter register. This sets the period. The other three are configured to set the match output to a one on a match. When CNT is reset, all match outputs are cleared. The output may or may not be inverted. This mode is useful to generate multiple pulses of varying length where one edge is coincident.

A sample PWM output is shown in Figure 8. In this example, match 0 is used for the period, while the outputs are match 1 through 3. Further, match 3 has been inverted.

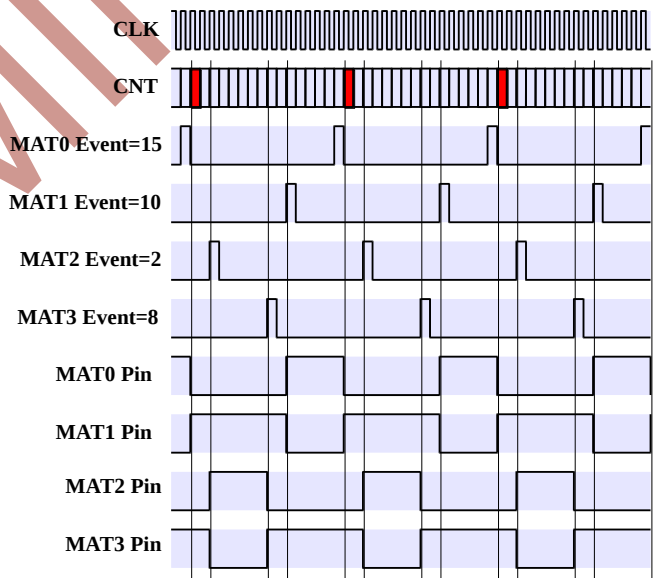

Figure 9: Timer/Counter Non-Overlapping Signals

Non-Overlapping Signals

A combination of match outputs can be used to set non-overlapping outputs. In this mode, match 0 and 1 events are used to generate the period and one of the pulses, while match 2 and 3 generate the other pulse. Match 0 is fixed for the period. Match 1 is used as the start time for one pulse. This pulse terminates at the end of the period. Match 2 and 3 are used to generate the second pulse. This pulse starts when there is a match 2, and ends when there is a match 3.

The match output pins are used as the non-overlap outputs. MAT0 is the positive pulse generated by match 0 and 1. MAT1 is the inverse of that signal. MAT2 is the positive pulse generated by match 2 and 3. MAT3 is the inverse of that signal. This example is shown in Figure 9.

Watchdog Timer

The watchdog timer is a 24-bit down counter. When it reaches 0, the microcontroller is reset or an interrupt is generated if enabled. It is reset with a feed sequence.

Real Time Counter

The real time counter can be used as a counter or a clock. The 32-bit counter increments by one each time the pre-scalar completes (binary mode). In the clock mode, the day, hour, minute, second, and 0.1 second value are output. The pre-scale register is a programmable, 32-bit system clock divisor.

EXTERNAL BUS

The external bus is an address/data multiplexed bus. The bus can be configured for eight-bit or thirty-two bit data. The bus uses up to thirty-two bits of address. The bus characteristics are:

- 32-bit address, 32 or 8-bit data
- Ninth bit (parity) for every byte
- Four programmable chip selects
- Byte enabled write (byte masking)
- Output enable for external devices
- Programmable latency, or driven by the WAIT pin
- Wired-or bus interrupt for external devices

SPECIFICATIONS

Absolute Maximums (1)

Temperature ..... -55 to 350ºC
Power Supply (V_{DD} referenced to ground) ..... -0.2 to 6.0 volts
Battery Voltage (V_{DDB} referenced to ground) ..... -0.2 to 6.0 volts
IO Voltage (referenced to ground) ..... -0.2 to 6.0 volts

1. Exceeding the maximum specifications may cause permanent damage to the part

Operating Conditions

Temperature (die) ..... -55 to 300ºC
Power Supply (V_{DD} referenced to ground) ..... 4.5 to 5.5 volts
Battery Voltage (V_{DDB} referenced to ground) ..... 3.4 to (V_{DD}+0.1) volts
IO Voltage (referenced to ground) ..... -0.2 to (V_{DD}+0.2) volts

DC Characteristics

Table 4: DC Characteristics (300C)

Symbol	Description	Min	Max @225C	Max @300C	Unit	Note
V_{DD}	Power Supply	4.5	5.5	5.5	V	
V_{DDB}	Battery Power Supply	3.4	V_{DD}-0.1	V_{DD}-0.1	V	
I_{DDs}	Static Current (no Clocking)		0.6	3	mA	
I_{DDB}	Battery Current (V_{DD}=0)		TBD	TBD	mA	(1)
V_{OH}	Output High Voltage (I_{OH}=2mA)	0.9*V_{DD}			V	
V_{OL}	Output Low Voltage (I_{OL}=2mA)		0.5	0.5	V	
V_{IH}	Input High Voltage	0.8*V_{DD}			V	
V_{IL}	Input Low Voltage		1.0	1.0	V	
I_I	Input Current		10	10	uA	
I_O	Output Current (in Tri-State)		10	10	uA	

Notes:

1. For systems not using battery backup, connect V_{DDB} to V_{DD}.

AC Characteristics

Table 5: AC Characteristics

Symbol	Description	Min	Max @225C	Max @300C	Unit	Note
f	Frequency	0	4	3.5	MHz	
t_{clkl}	CLK Low Time	100			ns	
t_{clkh}	CLK High Time	100			ns	
I_{DDA1}	Active Current (all Clocks Enabled)		14	14	mA/MHz	(1)
I_{DDA2}	Active Current (min Clocks Enabled)		7	8	mA/MHz	(1)
I_{DDA3}	Sleep Current (typical Clocks)		8	8	mA/MHz	(1)
I_{DDA4}	Deep Sleep Current (typical Clocks)		6	6	mA/MHz	(1)

Notes:

1. No Output Load.

Table 6: GPIO AC Characteristics (225C)

Symbol	Description	Min	Max @225C	Max @300C	Unit	Note
t_d	Output Delay		120	130	ns	
t_{dh}	Output Delay Hold	25			ns	
t_s	Input Setup Time	0			ns	
t_h	Input Hold Time	32			ns	
t_z	Delay to High-Z	20	130	130	ns	
t_e	Enable Delay		120	130	ns	

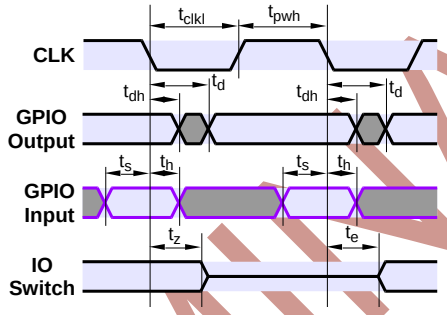

Figure 10: GPIO Timing

Table 7: CLKOUT AC Characteristics

Symbol	Description	Min	Max @225C	Max @300C	Unit	Note
t_{d1}	Output Delay, Divide by 1		105	120	ns	
t_d	Output Delay, Divide by > 1		100	110	ns	

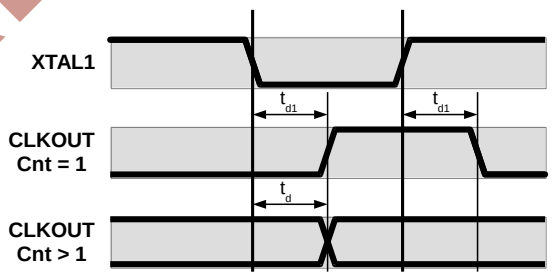

Figure 11: CLKOUT Timing

Table 8: Timer AC Characteristics

Symbol	Description	Min	Max @225C	Max @300C	Unit	Note
t_d	Match Output Delay		140	150	ns	
t_{dh}	Match Output Delay Hold	30			ns	
t_s	Capture Input Setup Time	0			ns	
t_h	Capture Input Hold Time	30			ns	

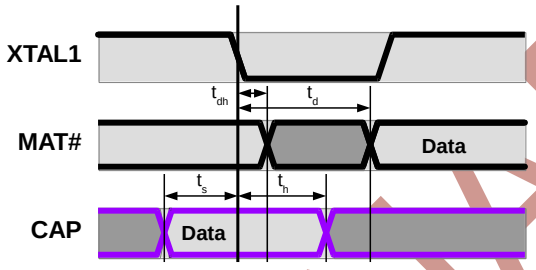

Figure 12: Timer Timing

Table 9: SPI AC Characteristics

Symbol	Description	Min	Max @225C	Max @300C	Unit	Note
t_d	MOSI Output Delay (SCLK)		0	0	ns	(1)
t_{dh}	MOSI Output Delay Hold (SCLK)	-55			ns	(1)
t_s	MISO Input Setup Time (SCLK)	150			ns	
t_h	MISO Input Hold Time (SCLK)	0			ns	

Note:

1. To/From Data Clock Edge, not Active Sample Edge.

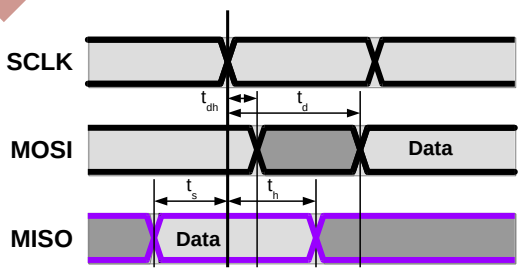

Figure 13: SPI Timing

Table 10: External Bus AC Characteristics

Symbol	Description	Min	Max @225C	Max @300C	Unit	Note
t_{da}	ADQ Address Output Delay		75	80	ns	
t_{dav}	ADVN Output Delay		60	65	ns	
t_{dbw}	BWN Output Delay		60	65	ns	
t_{dcr}	CRE Output Delay		60	65	ns	
t_{dcs}	CSN Output Delay		75	80	ns	
t_{dd}	ADQ Data Output Delay		75	80	ns	
t_{doe}	OEN Output Delay		60	65	ns	
t_{dp}	PDQ Output Delay		75	80	ns	
t_{dwe}	WEN Output Delay		60	65	ns	
t_{dha}	ADQ Address Output Hold	5			ns	
t_{dhav}	ADVN Output Hold	5			ns	
t_{dhbw}	BWN Output Hold	5			ns	
t_{dhcr}	CRE Output Hold	5			ns	
t_{dhcs}	CSN Output Hold	5			ns	
t_{dhd}	ADQ Data Output Hold	5			ns	
t_{dhoe}	OEN Output Hold	5			ns	
t_{dp}	PDQ Output Hold	5			ns	
t_{dhwe}	WEN Output Hold	5			ns	
t_{sd}	ADQ Data Input Setup Time	80			ns	
t_{sp}	PDQ Input Setup Time	80			ns	
t_{sw}	WAIT Input Setup Time	90			ns	
t_{hd}	ADQ Data Input Hold Time	0			ns	
t_{hp}	PDQ Input Hold Time	0			ns	
t_{hw}	WAIT Input Hold Time	0			ns	
t_{za}	ADQ Address Delay to High-Z	10	60	65	ns	
t_{zp}	PDQ Delay to High-Z	10	60	65	ns	
t_{ea}	ADQ Address Enable Delay		50	55	ns	
t_{ep}	PDQ Enable Delay		50	55	ns	

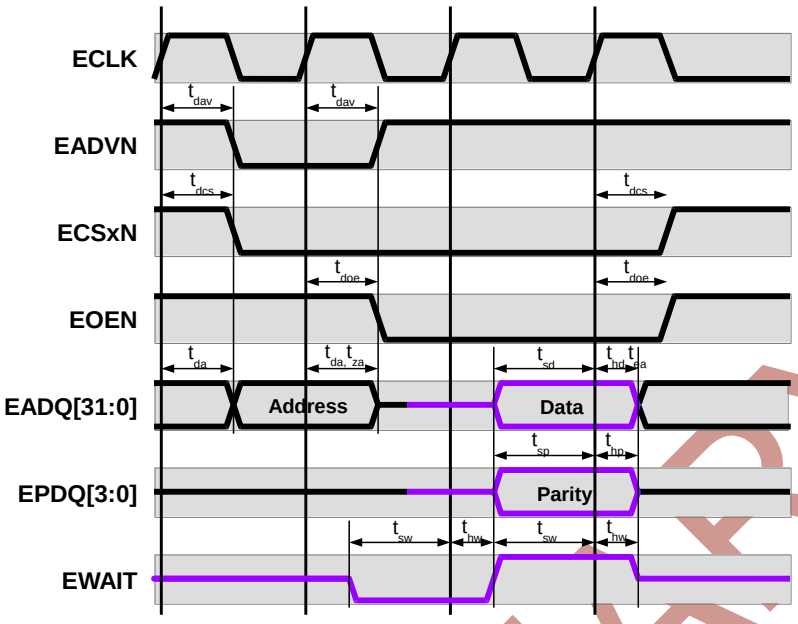

Figure 14: 32-bit Read, 1 Cycle Latency

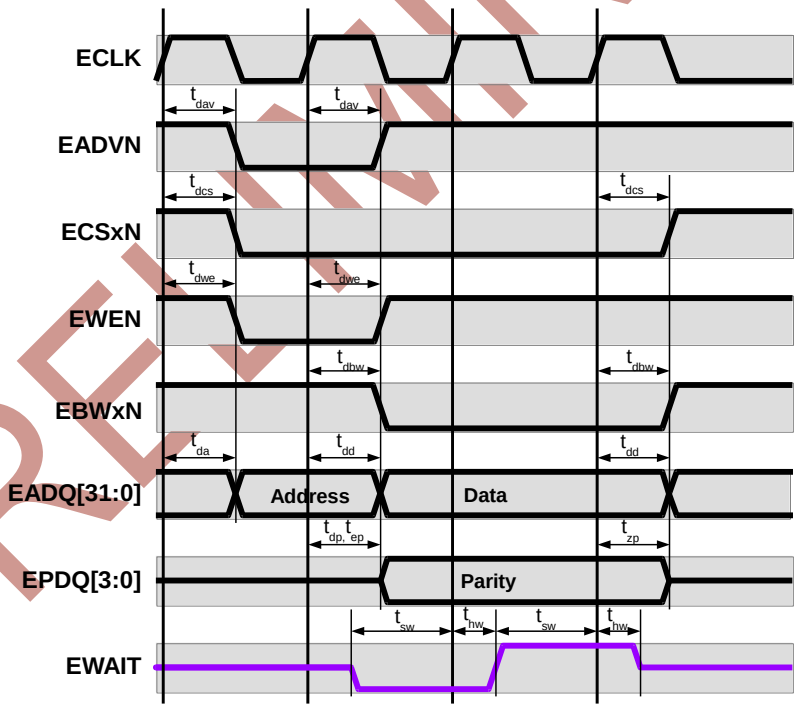

Figure 15: 32-bit Write, 1 Cycle Latency

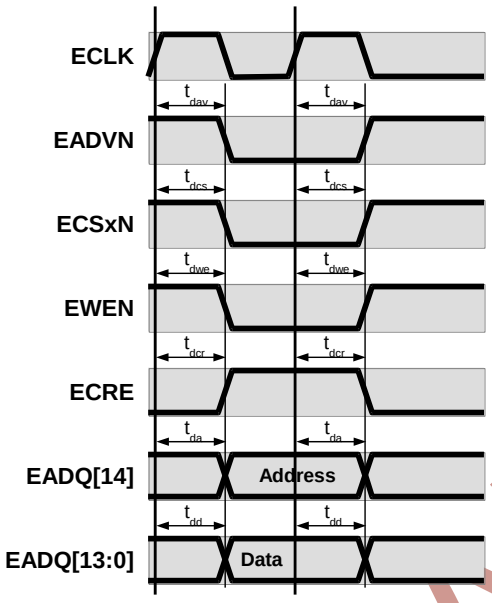

Figure 16: Configuration Write

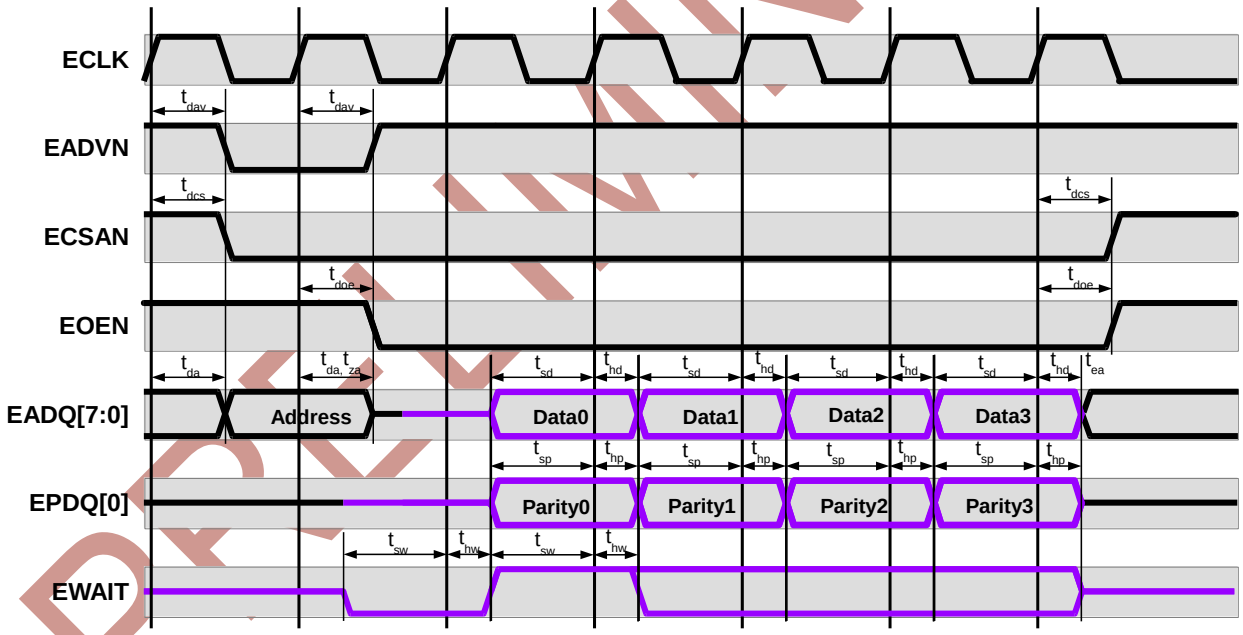

Figure 17: 8-bit Read, One Cycle Latency

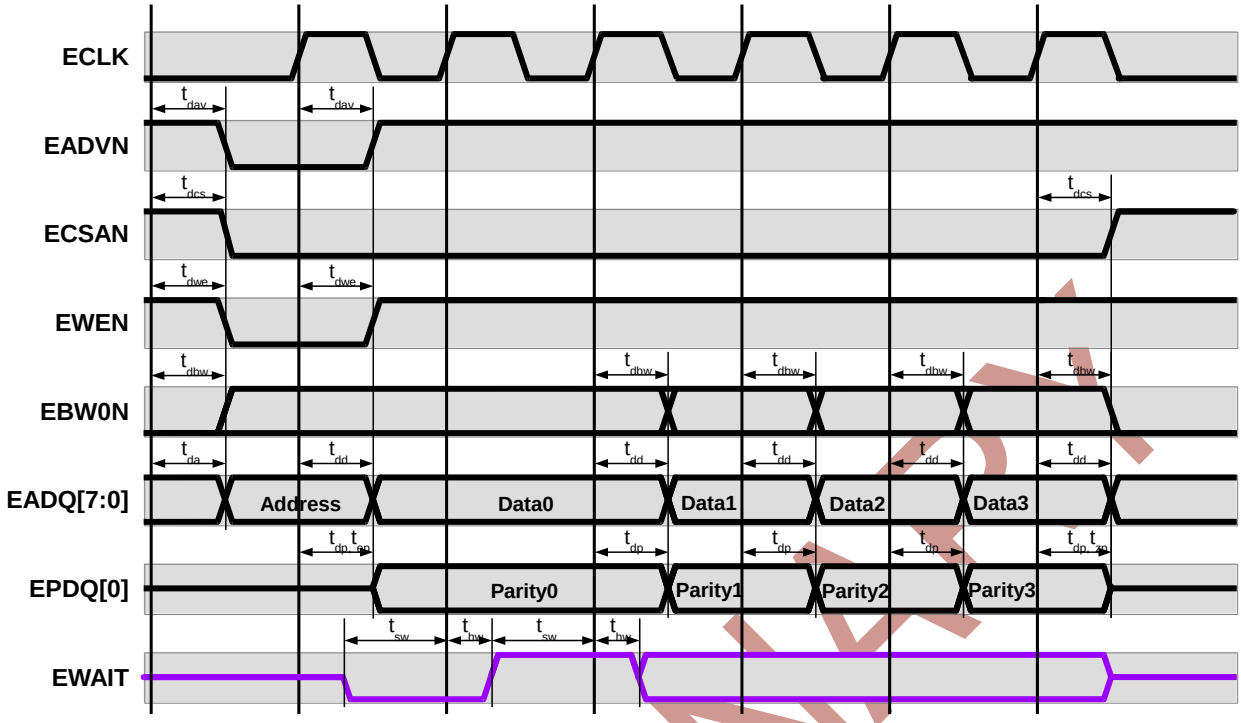

Figure 18: 8-bit Write, One Cycle Latency

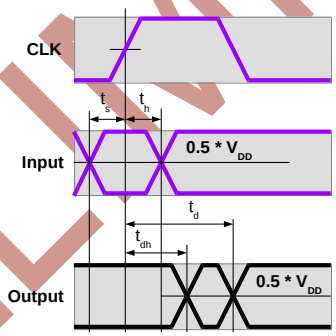

Figure 19: Delay Measurement

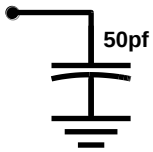

Figure 20: AC Load

PACKAGING

The RC10001 is packaged as a 144 pin QFP.

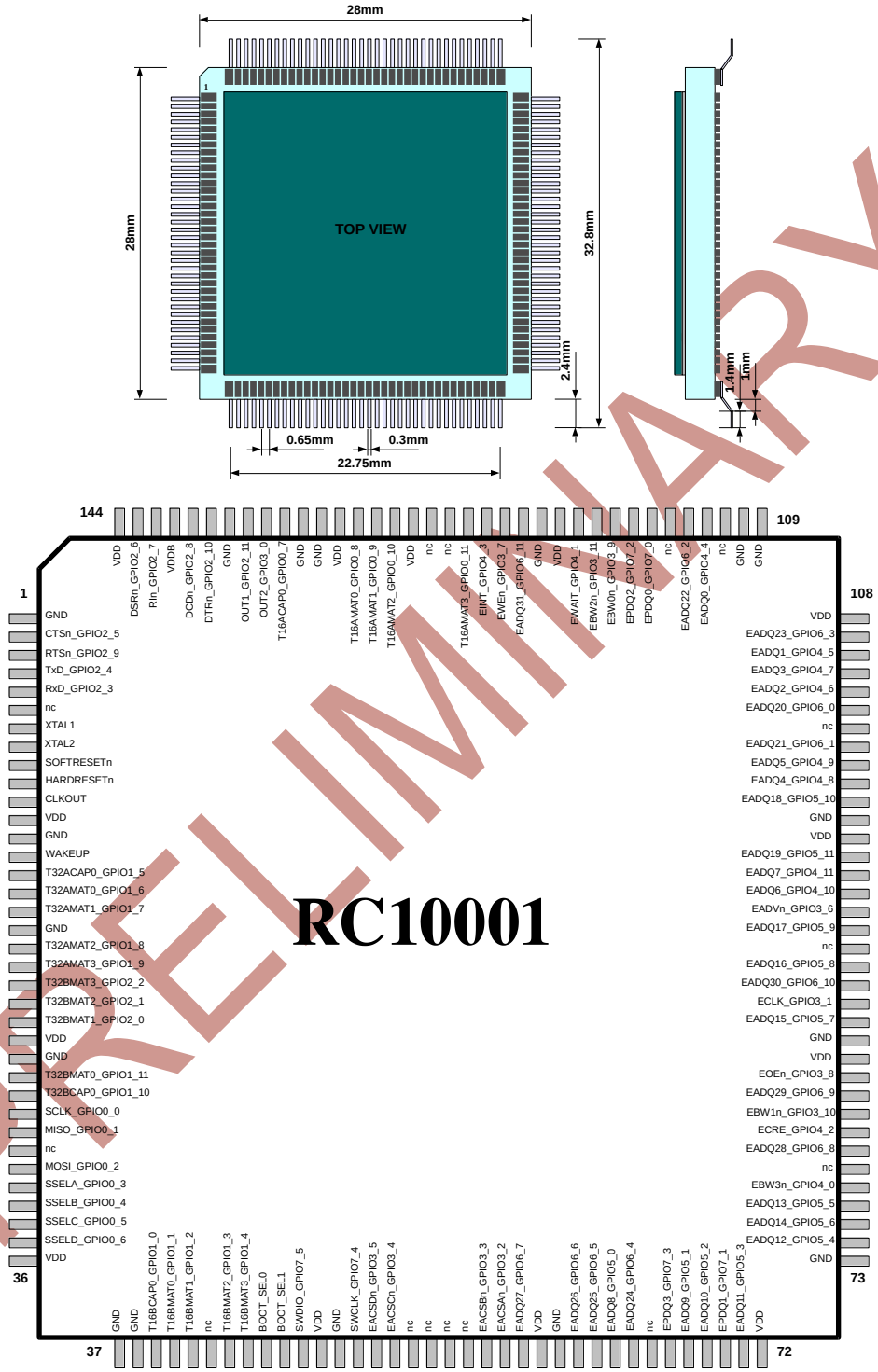

Figure 21: 144-Pin QFP Package

Table 11: Pin Out

Pin	Symbol	Type	Default	Function	Pin	Symbol	Type	Default	Description
1	GND	PWR	na	Ground	73	GND	PWR	na	Ground
2	CTSn_GPIO2_5	I/O	I: PU	UART: Clear to Send	74	EADQ12_GPIO5_4	I/O	I: PU	External Address/Data
3	RTSn_GPIO2_9	I/O	I: PU	UART: Request to Send	75	EADQ14_GPIO5_6	I/O	I: PU	External Address/Data
4	TxD_GPIO2_4	I/O	I: PU	UART: Transmit Data	76	EADQ13_GPIO5_5	I/O	I: PU	External Address/Data
5	RxD_GPIO2_3	I/O	I: PU	UART: Receive Data	77	EBW3n_GPIO4_0	I/O	I: PU	External Byte Write
6	nc	na	na	No Connect	78	nc	na	na	No Connect
7	XTAL1	I	na	Oscillator Input	79	EADQ28_GPIO6_8	I/O	I: PU	External Address/Data
8	XTAL2	O	na	Oscillator Output	80	ECRE_GPIO4_2	I/O	I: PU	External Control Register
9	SOFTRESETn	I	I: PU	Reset	81	EBW1n_GPIO3_10	I/O	I: PU	External Byte Write
10	HARDRESETn	I	I: PU	Reset	82	EADQ29_GPIO6_9	I/O	I: PU	External Address/Data
11	CLKOUT	O	O	Clock Output	83	EOEn_GPIO3_8	I/O	I: PU	External Output Enable
12	VDD	PWR	na	Power	84	VDD	PWR	na	Power
13	GND	PWR	na	Ground	85	GND	PWR	na	Ground
14	WAKEUP	I	I: PU	Wakeup	86	EADQ15_GPIO5_7	I/O	I: PU	External Address/Data
15	T32ACAP0_GPIO1_5	I/O	I: PU	T32 Capture	87	ECLK_GPIO3_1	I/O	I: PU	External Clock
16	T32AMAT0_GPIO1_6	I/O	I: PU	T32 Match	88	EADQ30_GPIO6_10	I/O	I: PU	External Address/Data
17	T32AMAT1_GPIO1_7	I/O	I: PU	T32 Match	89	EADQ16_GPIO5_8	I/O	I: PU	External Address/Data
18	nc	na	na	No Connect	90	nc	na	na	No Connect
19	T32AMAT2_GPIO1_8	I/O	I: PU	T32 Match	91	EADQ17_GPIO5_9	I/O	I: PU	External Address/Data
20	T32AMAT3_GPIO1_9	I/O	I: PU	T32 Match	92	EADVn_GPIO3_6	I/O	I: PU	External Address Valid
21	T32BMAT3_GPIO2_2	I/O	I: PU	T32 Match	93	EADQ6_GPIO4_10	I/O	I: PU	External Address/Data
22	T32BMAT2_GPIO2_1	I/O	I: PU	T32 Match	94	EADQ7_GPIO4_11	I/O	I: PU	External Address/Data
23	T32BMAT1_GPIO2_0	I/O	I: PU	T32 Match	95	EADQ19_GPIO5_11	I/O	I: PU	External Address/Data
24	VDD	PWR	na	Power	96	VDD	PWR	na	Power
25	GND	PWR	na	Ground	97	GND	PWR	na	Ground
26	T32BMAT0_GPIO1_11	I/O	I: PU	T32 Match	98	EADQ18_GPIO5_10	I/O	I: PU	External Address/Data
27	T32BCAP0_GPIO1_10	I/O	I: PU	T32 Match	99	EADQ4_GPIO4_8	I/O	I: PU	External Address/Data
28	SCLK_GPIO0_0	I/O	I: PU	SPI Clock	100	EADQ5_GPIO4_9	I/O	I: PU	External Address/Data
29	MISO_GPIO0_1	I/O	I: PU	SPI Master In	101	EADQ21_GPIO6_1	I/O	I: PU	External Address/Data
30	nc	na	na	No Connect	102	nc	na	na	No Connect
31	MOSI_GPIO0_2	I/O	I: PU	SPI Master Out	103	EADQ20_GPIO6_0	I/O	I: PU	External Address/Data
32	SSELA_GPIO0_3	I/O	I: PU	SPI Select	104	EADQ2_GPIO4_6	I/O	I: PU	External Address/Data
33	SSELB_GPIO0_4	I/O	I: PU	SPI Select	105	EADQ3_GPIO4_7	I/O	I: PU	External Address/Data
34	SSELC_GPIO0_5	I/O	I: PU	SPI Select	106	EADQ1_GPIO4_5	I/O	I: PU	External Address/Data
35	SSELD_GPIO0_6	I/O	I: PU	SPI Select	107	EADQ23_GPIO6_3	I/O	I: PU	External Address/Data
36	VDD	PWR	na	Power	108	VDD	PWR	na	Power
37	GND	PWR	na	Ground	109	GND	PWR	na	Ground
38	GND	PWR	na	Ground	110	GND	PWR	na	Ground
39	T16BCAP0_GPIO1_0	I/O	I: PU	T16 Capture	111	nc	na	na	No Connect
40	T16BMAT0_GPIO1_1	I/O	I: PU	T16 Match	112	EADQ0_GPIO4_4	I/O	I: PU	External Address/Data
41	T16BMAT1_GPIO1_2	I/O	I: PU	T16 Match	113	EADQ22_GPIO6_2	I/O	I: PU	External Address/Data
42	nc	na	na	No Connect	114	nc	na	na	No Connect
43	T16BMAT2_GPIO1_3	I/O	I: PU	T16 Match	115	EPDQ0_GPIO7_0	I/O	I: PU	External Address/Data
44	T16BMAT3_GPIO1_4	I/O	I: PU	T16 Match	116	EPDQ2_GPIO7_2	I/O	I: PU	External Address/Data
45	BOOT_SEL0	I	I: PD	Boot Select	117	EBW0n_GPIO3_9	I/O	I: PU	External Byte Write
46	BOOT_SEL1	I	I: PD	Boot Select	118	EBW2n_GPIO3_11	I/O	I: PU	External Byte Write
47	SWDIO_GPIO7_5	I/O	I: PD	Serial Wire Data	119	EWAIT_GPIO4_1	I/O	I: PU	External Wait for Slave
48	VDD	PWR	Na	Power	120	VDD	PWR	Na	Power
49	GND	PWR	Na	Ground	121	GND	PWR	Na	Ground
50	SWCLK_GPIO7_4	I/O	I: PD	Serial Wire Clock	122	EADQ31_GPIO6_11	I/O	I: PU	External Address/Data
51	EACSDn_GPIO3_5	I/O	I: PU	External Chip Select	123	EWEn_GPIO3_7	I/O	I: PU	External Write
52	EACSCn_GPIO3_4	I/O	I: PU	External Chip Select	124	EINT_GPIO4_3	I/O	I: PU	External Interrupt
53	nc	na	na	No Connect	125	T16AMAT3_GPIO0_11	I/O	I: PU	T16 Match
54	nc	na	na	No Connect	126	nc	na	na	No Connect
55	nc	na	na	No Connect	127	nc	na	na	No Connect
56	nc	na	na	No Connect	128	VDD	PWR	na	Power
57	EACSBn_GPIO3_3	I/O	I: PU	External Chip Select	129	T16AMAT2_GPIO0_10	I/O	I: PU	T16 Match
58	EACSAn_GPIO3_2	I/O	I: PU	External Chip Select	130	T16AMAT1_GPIO0_9	I/O	I: PU	T16 Match
59	EADQ27_GPIO6_7	I/O	I: PU	External Address/Data	131	T16AMAT0_GPIO0_8	I/O	I: PU	T16 Match
60	VDD	PWR	na	Power	132	VDD	PWR	na	Power
61	GND	PWR	na	Ground	133	GND	PWR	na	Ground
62	EADQ26_GPIO6_6	I/O	I: PU	External Address/Data	134	GND	PWR	na	Ground
63	EADQ25_GPIO6_5	I/O	I: PU	External Address/Data	135	T16ACAP0_GPIO0_7	I/O	I: PU	T16 Capture
64	EADQ8_GPIO5_0	I/O	I: PU	External Address/Data	136	OUT2_GPIO3_0	I/O	I: PU	UART Output
65	EADQ24_GPIO6_4	I/O	I: PU	External Address/Data	137	OUT1_GPIO2_11	I/O	I: PU	UART Output
66	nc	na	na	No Connect	138	GND	PWR	na	Ground
67	EPDQ3_GPIO7_3	I/O	I: PU	External Address/Data	139	DTRn_GPIO2_10	I/O	I: PU	UART Data Terminal
68	EADQ9_GPIO5_1	I/O	I: PU	External Address/Data	140	DCDn_GPIO2_8	I/O	I: PU	UART Carrier Detect
69	EADQ10_GPIO5_2	I/O	I: PU	External Address/Data	141	VDDB	PWR	na	Battery Power
70	EPDQ1_GPIO7_1	I/O	I: PU	External Address/Data	142	RIn_GPIO2_7	I/O	I: PU	UART Ring
71	EADQ11_GPIO5_3	I/O	I: PU	External Address/Data	143	DSRn_GPIO2_6	I/O	I: PU	UART Data Set
72	VDD	PWR	na	Power	144	VDD	PWR	na	Power

Definitions for the pin out table above:

I – input

O – output

I/O - bi-directional input or output

PU – weak pull-up transistor connected to the output

PD- weak pull-down transistor connected to the output