FEATURES

- **-55°C to 300°C Temperature Range**
- 32K x 9 Random Access Memory
- 5-volt Operation
- 3.4-volt Battery Back Up
- Fully Static Design
- Parity Options
  - 8-Bit Data
  - 9-Bit Data
  - Even Parity
  - Odd Parity
  - Parity Error Bit

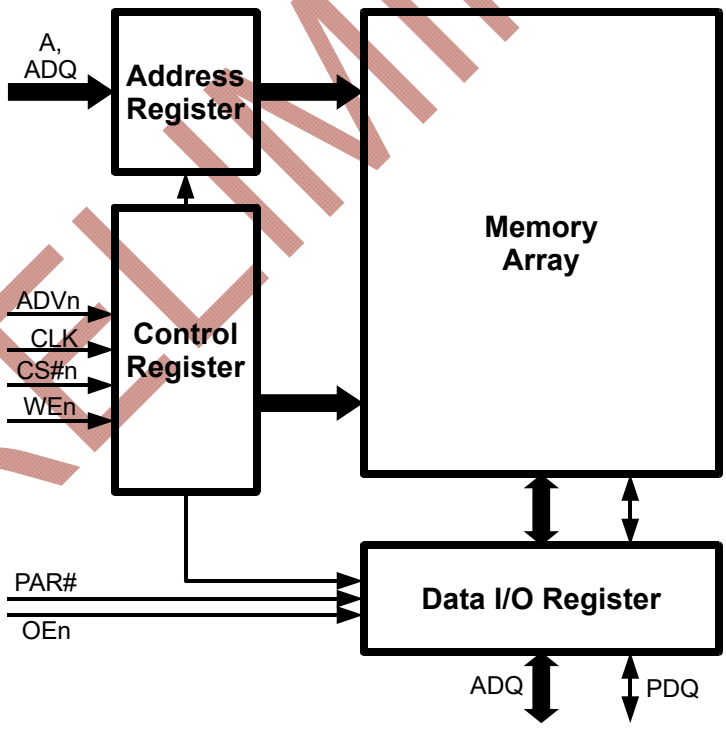


Figure 1: Block Diagram

DESCRIPTION

The RelChip® RC2103209 is a synchronous 32Kx9 RAM. The part uses a multiplexed bus (address and data). Ninth bit or parity is selected by pin configuration.

Fifteen bits of address are provided during the address cycle. Eight bits of data plus parity are transferred in the data cycle.

Parity Configuration

The ninth data bit (on the PDQ pin) is configured for data or parity by the PAR0 through PAR2 pins. These pins should all be tied high or low as required. Table 1 shows the available configurations.

For even and odd parity modes, parity is calculated on the eight bits during a write, and stored with the data. When read, the data is reported and PDQ outputs the parity bit.

In the parity error mode, parity is calculated and written to memory during a write. However, during a read operation, the parity is calculated on the read data and compare to the parity previously written. Parity errors are reported on the PDQ pin.

Table 1: Parity Selections

PAR[2:0]	PDQ Input	PDQ Output
000	GND(1)	na
001	Data Bit 9	Data Bit 9
010	na	Even Parity
011	na	Odd Parity
1xx	na	Parity Error

Read

Read occurs when WEn is not asserted, and an address cycle starts. During the address cycle, the address is issued to the part. On the next cycle, the read data is available.

Write

Write occurs when WEn is asserted, and an address cycle starts. During the address cycle, the address is issued to the part. On the next cycle, the write data is issued.

SPECIFICATIONS

Absolute Maximums (1)

Temperature ..... -55 to 350ºC
Power Supply (V_{DD} referenced to ground) ..... -0.2 to 6.0 volts
Battery Voltage (V_{DDB} referenced to ground) ..... -0.2 to 6.0 volts
IO Voltage (referenced to ground) ..... -0.2 to 6.0 volts

1. Exceeding the maximum specifications may cause permanent damage to the part

Operating Conditions

Temperature (die temperature) ..... -55 to 300ºC
Power Supply (V_{DD} referenced to ground) ..... 4.5 to 5.5 volts
Battery Voltage (V_{DDB} referenced to ground) ..... 3.4 to (V_{DD}+0.1) volts
IO Voltage (referenced to ground) ..... 0.2 to (V_{DD}+0.2) volts

DC Characteristics

Table 2: DC Characteristics

Symbol	Description	Min	Typ	Max @225C	Max @300C	Unit	Note
T	Temperature	-55	25	225	300	ºC	
V_{DD}	Digital Power Supply	4.5	5	5.5	5.5	V	
V_{DDB}	Battery Power Supply	3.4		V_{DD}+0.1	V_{DD}+0.1	V	1
I_{DD}	Active Current			2.5	3	mA/MHz	2
I_{DD}	Standby Current (CSn = V_{DD})			1.5	2	mA/MHz	2,3
I_{DDB}	Battery Current (V_{DD}=0)			0.005	8	mA	4
V_{OH}	Output High Voltage (I_{OH}=2mA)	0.9*V_{DD}				V	
V_{OL}	Output Low Voltage (I_{OL}=2mA)			0.5	0.5	V	
V_{IH}	Input High Voltage	0.8*V_{DD}				V	
V_{IL}	Input Low Voltage			1.0	1.0	V	
I_I	Input Current			10	10	uA	

Notes:

1. For systems not using battery backup, connect the VDDB pin to VDD.
2. No Output Load.
3. All bus signals toggling simulating other memories on the bus.
4. When not running on the battery, this DC current must be added to active and standby currents.

AC Characteristics

Table 3: AC Characteristics

Symbol	Description	Min	Max @225C	Max @300C	Unit	Note
F	Frequency		5	4	MHz	
t_{pw}	Pulse Width: CLK	80			nS	
t_{dd}	Delay: CLK ↑ to ADQ		120	130	nS	
t_{dp}	Delay: CLK ↑ to PDQ		120	130	nS	
t_{dhd}	Hold: ADQ after CLK ↑	20	100	110	nS	
t_{dhp}	Hold: PDQ after CLK ↑	20	100	110	nS	
t_{ed}	Enable: OEn ↓ to ADQ	TBD	TBD	TBD	nS	
t_{ep}	Enable: OEn ↓ to PDQ	TBD	TBD	TBD	nS	
t_{zd}	Disable: OEn ↑ ADQ	TBD	TBD	TBD	nS	
t_{zp}	Disable: OEn ↑ PDQ	TBD	TBD	TBD	nS	
t_{sa}	Setup: ADQ/A to CLK ↑	3			nS	
t_{sav}	Setup: ADVn ↓ to CLK ↑	3			nS	
t_{scs}	Setup: CSn ↓ to CLK ↑	TBD			nS	
t_{sd}	Setup: ADQ to CLK ↑	3			nS	
t_{sp}	Setup: PDQ to CLK ↑	3			nS	
t_{swe}	Setup: WEn to CLK ↑	3			nS	
t_{ha}	Hold: ADQ/A from CLK ↑	15			nS	
t_{hav}	Hold: ADVn ↑ from CLK ↑	15			nS	
t_{hcs}	Hold: CSn ↑ from CLK ↑	TBD			nS	
t_{hd}	Hold: ADQ from CLK ↑	15			nS	
t_{hp}	Hold: PDQ from CLK ↑	15			nS	
t_{hwe}	Hold: WEn from CLK ↑	5			nS	

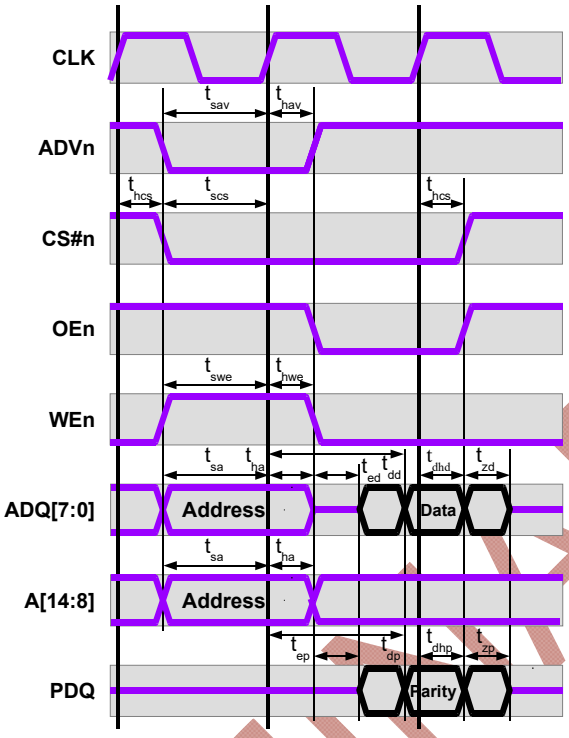


Figure 2: Read Timing

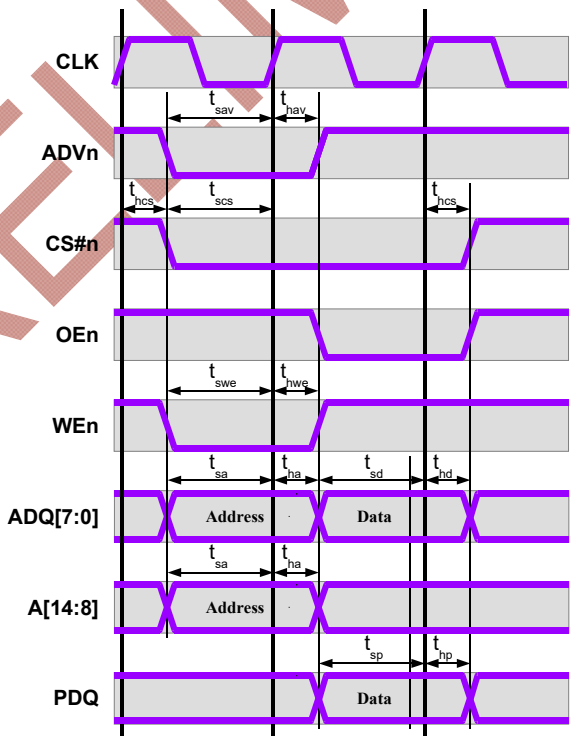


Figure 3: Write Timing

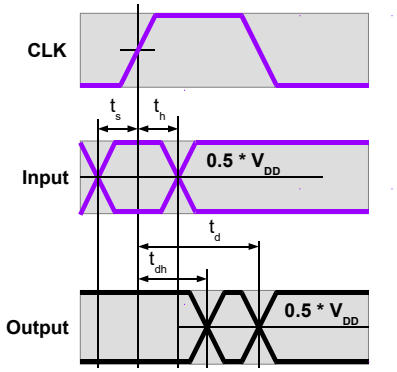


Figure 4: Delay Measurement

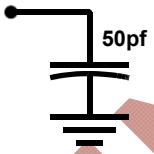
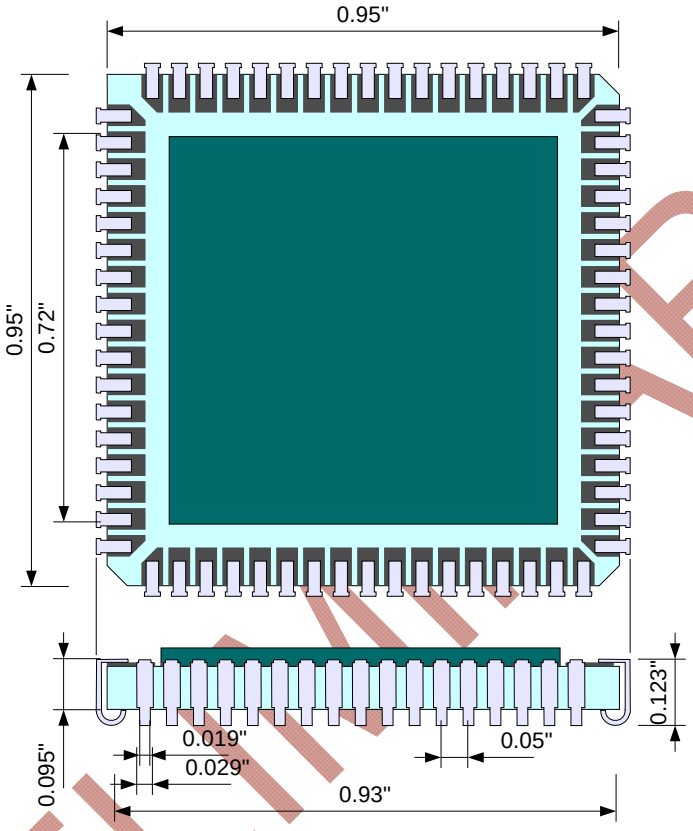


Figure 5: AC Measurement Load

PACKAGING

The RC2103209 is packaged in a 68 pin J-Lead QFP.



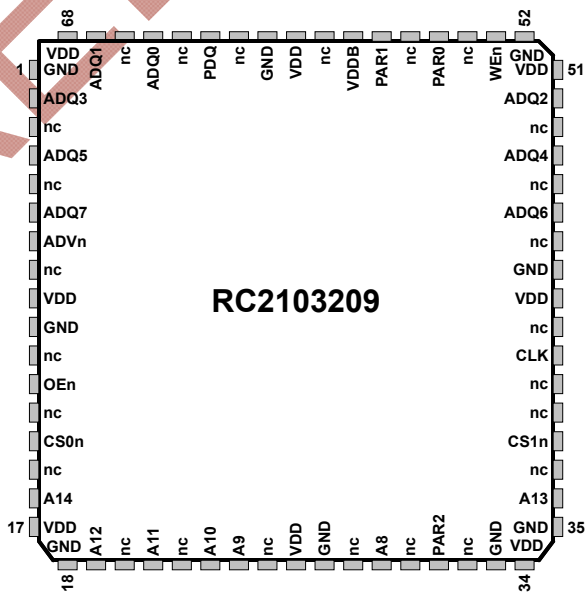


Table 4: Pin Out

Pin	Name	Dir	Function	Pin	Name	Dir	Function
1	GND	GND	Ground	35	GND	GND	Ground
2	ADQ3	IO	Address/Data	36	A13	In	Address Input
3	nc	na	No Connection	37	nc	na	No Connection
4	ADQ5	IO	Address/Data	38	CS1n	In	Chip Enable
5	nc	na	No Connection	39	nc	na	No Connection
6	ADQ7	IO	Address/Data	40	nc	na	No Connection
7	ADVn	In	Address Valid	41	CLK	In	Clock
8	nc	na	No Connection	42	nc	na	No Connection
9	VDD	VDD	Power Supply	43	VDD	VDD	Power Supply
10	GND	GND	Ground	44	GND	GND	Ground
11	nc	na	No Connection	45	nc	na	No Connection
12	OEn	In	Output Enable	46	ADQ6	IO	Address/Data
13	nc	na	No Connection	47	nc	na	No Connection
14	CS0n	In	Chip Enable	48	ADQ4	IO	Address/Data
15	nc	na	No Connection	49	nc	na	No Connection
16	A14	In	Address Input	50	ADQ2	IO	Address/Data
17	VDD	VDD	Power Supply	51	VDD	VDD	Power Supply
18	GND	GND	Ground	52	GND	GND	Ground
19	A12	In	Address Input	53	WEn	Input	Write Select
20	nc	na	No Connection	54	nc	na	No Connection
21	A11	Input	Address Input	55	PAR0	Input	Parity Select
22	nc	na	No Connection	56	nc	na	No Connection
23	A10	Input	Address Input	57	PAR1	Input	Parity Select
24	A9	Input	Address Input	58	VDDB	VDDB	Battery Backup
25	nc	na	No Connection	59	nc	na	No Connection
26	VDD	VDD	Power Supply	60	VDD	VDD	Power Supply
27	GND	GND	Ground	61	GND	GND	Ground
28	nc	na	No Connection	62	nc	na	No Connection
29	A8	In	Address Input	63	PDQ	IO	Parity
30	nc	na	No Connection	64	nc	na	No Connection
31	PAR2	In	Parity Mode	65	ADQ0	IO	Address/Data
32	nc	na	No Connection	66	nc	na	No Connection
33	GND	GND	Ground	67	ADQ1	IO	Address/Data
34	VDD	VDD	Power Supply	68	VDD	VDD	Power Supply