FEATURES

- **-55°C to 300°C Temperature Range**
- 8K x 36 Random Access Memory
- 5-volt Operation
- 3.4-volt Battery Back Up
- Fully Static Design
- Parity Options
  - 8-Bit Data
  - 9-Bit Data
  - Even, Odd, or Sticky Parity
  - Parity Error
- Burst (4 word) or Single Operations
- RC10001 Compatible

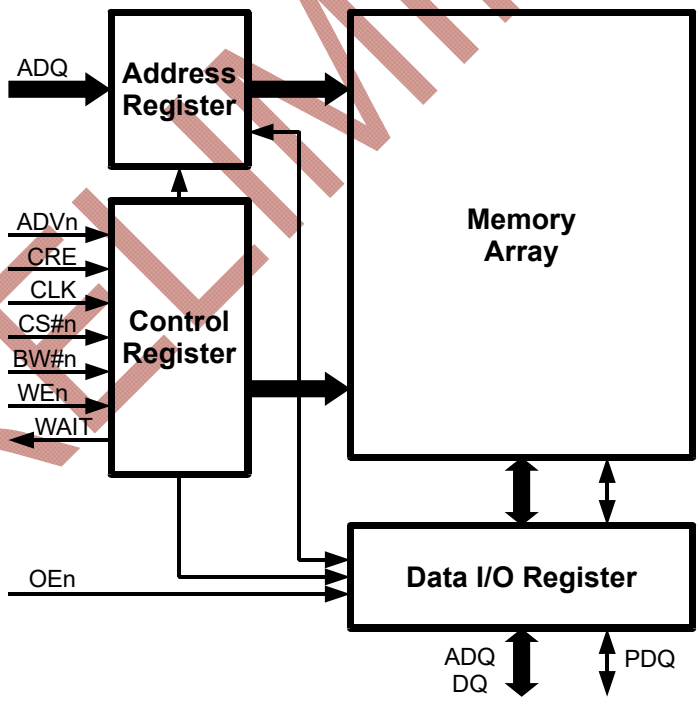


Figure 1: Block Diagram

DESCRIPTION

The RelChip® RC2110836 is a synchronous 8Kx36 RAM compatible with the RC10001 microcontroller. The memory is highly configurable, with options for data width, parity, latency, and burst-mode. Each byte of the 32 data pins can be written individually with the byte write (BW0n through BW3n) control pins.

Thirteen bits of address (ADQ [14:2]) are input during the address cycle. The data is word aligned.

Configuration

Product configuration is set by programming the configuration register (see Table 1). The memory array is 36 bits wide. 32 bits are data and the other 4 can be configured to be either data or parity. Parity bits are configured even, odd, or parity error. Latency, or the number of cycles from the address cycle to the data cycle, is programmable from one to eight cycles. A single address cycle can trigger a read or write of four words in the burst mode.

Configuration Register

The configuration consists of two registers of fourteen bits selected by A [14] (see Table 1). A special configuration write operation (Figure 2) is used to set the configuration. The first register stores the latency and burst configuration, while the second stores the parity configuration.

Table 1: Configuration Register

A [14]	Bit	Symbol	Description	Default
0	13:11	Latency Count	Data Available in n+1 Clocks (See Table 2)	010
0	10:1	Reserved	Reserved	-
0	0	Burst Length	0=1, 1=4	0
1	13:3	Reserved	Reserved	-
1	2:0	Parity Selection	Parity Mode (See Table 3)	000

Latency

Latency can be programmed from one to eight cycles (see Table 1 and Table 2). Latency is the number of clock cycles from the address cycle to the data cycle (either read or write, Figure 3). Latency is configured with bits 13 through 11 of the first configuration register. The default value is three cycles.

Table 2: Latency Selections

Value (binary)	Latency (cycles)	default
000	1	
001	2	
010	3	X
011	4	
100	5	
101	6	
110	7	
111	8	

Burst Mode

The RC2110836 can execute one or four read or write operations for each address cycle. This mode is set in the configuration register (see Table 1). Burst operations begin at the address specified during the address cycle (A[14:2]). Subsequent operations occur at the next address (modulo 4). If the operation is started with A [3:2] set to “00,” the part will use that address for the first operation, followed by “01,” “10,” and “11.” However, if the operations begin at A[3:2] equal to “10,” the sequence would then follow as “11,” “00,” and “01.” This operation will not modify A[4]. A burst operation is aborted or ended by deselecting the part (CS0n or CS1n go high). An abort will not roll-back previous write operations. A burst will continue (with address wrapping) until the part is deselected.

Parity

The parity IO is configured through bits 2:0 in the configuration register (see Table 1 and Table 3). The parity IO pins can be configured to floating, data, parity, or parity error. If they are not used, the pins should be configured to float, and be tied to ground externally.

The RC2110836 can be configured as a 32-bit part with parity, or as a by 36-bit part without parity. As a 32-bit part, the parity IO pins are byte parity pins for the four bytes in a word. For 36-bit operation, the parity IO pins (PDQ0 through PDQ3) are used for data.

The RC2110836 will calculate the parity for each written byte (D[7:0], D[15:8], D[23:16], and D[31:24]), storing the values in the parity bits (P[0] through P[3] respectively). The parity mode is set in the configuration. For all parity modes, the 4 bits are calculated and stored in memory.

When the part is read in even or odd parity modes, the parity value calculated during the write is reported on the PDQ pins. If the part is read in the parity error mode, the four bytes read have a new parity calculated. The PDQ pin is asserted when this new parity value is different than the stored one.

Table 3: Parity Selections

Value (binary)	Parity Bit (PDQ)	default
000	Z	
001	Nine Bit Data	X
010	Even Parity	
011	Odd Parity	
1xx	Parity Error	

Status Register

There are, like the configuration register, two status registers. These are full 32-bit registers (see Table 4). The status includes all the configuration bits plus product identification fields.

Table 4: Status Register Contents

A [14]	Register	Symbol	Description	Constant
0	31:14	Reserved	Reserved	0
0	13:11	Latency Count	Data Available in n+1 Clocks (See Table 2)	
0	10:1	Reserved	Reserved	1010100
0	0	Burst Length	0=1, 1=4	
1	31:16	Part Number	Integer	0x07D0
1	15:14	Reserved	Reserved	00
1	13:10	Configuration	Integer	0101
1	9:3	Revision Number	Integer	0000100
1	2:0	Parity Selection	Parity Mode (See Table 3)	

Configuration Write

Configuration writes always occur in a single cycle (Figure 2). With the Configuration Register Enable pin (CRE) asserted high, a write operation is initiated. Address input 14 selects which of the two configuration registers is addressed. Address inputs 13 through 0 set the configuration bits.

Status Read

A status read is identical to a normal read except that the CRE pin is asserted high. The parity bit is always output as a low during a status read if enabled.

Read and Write with Latency

Adding latency to operations, whether burst mode or not, just adds cycles between the address cycle and the first operation cycle.

SPECIFICATIONS

Absolute Maximums (1)

Temperature ..... -55 to 350ºC
Power Supply (V_{DD} referenced to ground) ..... -0.2 to 6.0 volts
Battery Voltage (V_{DDB} referenced to ground) ..... -0.2 to 6.0 volts
IO Voltage (referenced to ground) ..... -0.2 to 6.0 volts

Operating Conditions

Temperature (die temperature) ..... -55 to 300ºC
Power Supply (V_{DD} referenced to ground) ..... 4.5 to 5.5 volts
Battery Voltage (V_{DDB} referenced to ground) ..... 3.4 to (V_{DD}+0.1) volts
IO Voltage (referenced to ground) ..... -0.2 to (V_{DD}+0.2) volts

1. Exceeding the maximum specifications may cause permanent damage

DC Characteristics

Table 5: DC Characteristics (225C)

Symbol	Description	Min	Max @225C	Max @300C	Unit	Note
T	Temperature	-55	225	300	ºC	
V_{DD}	Digital Power Supply	4.5	5.5	5.5	V	
V_{DDB}	Battery Power Supply	3.4	V_{DD}+0.1	V_{DD}+0.1	V	1
I_{DD}	Active Current		2.5	3	mA/MHz	2
I_{DDS}	Standby Current (CSn=V_{DD})		1.5	2	mA/MHz	2,3
I_{DDB}	Battery Current (V_{DD}=0)		0.005	8	mA	4
V_{OH}	Digital Output High Voltage (I_{OH}=2mA)	0.9*V_{DD}			V	
V_{OL}	Digital Output Low Voltage (I_{OL}=2mA)		0.5	0.5	V	
V_{IH}	Digital Input High Voltage	0.8*V_{DD}			V	
V_{IL}	Digital Input Low Voltage		1.0	1.0	V	
I_I	Digital Input Current		10	10	uA	

Notes:

1. For systems not using battery backup, connect VDDB to VDD.
2. No Output Load.
3. All bus signals toggling simulating other memories on the bus.
4. When running on VDD, this DC current must be added to active and standby currents.

AC Characteristics

Table 6: AC Characteristics

Symbol	Description	Min	Max @225C	Max @300C	Unit	Note
f	Frequency		5	4	MHz	
t_{pw}	Pulse Width: CLK	80			nS	
t_{dd}	Delay: ADQ/DQ from CLK ↑		120	130	nS	
t_{dp}	Delay: PDQ from CLK ↑		120	130	nS	
t_{dw}	Delay: WAIT from CLK		75	80	nS	
t_{dhd}	Hold: DQ after CLK ↑	20	100	110	nS	
t_{dhp}	Hold: PDQ after CLK ↑	20	100	110	nS	
t_{ed}	Enable: DQ after OEn ↓	TBD	TBD	TBD	nS	
t_{ep}	Enable: PDQ after OEn ↓	TBD	TBD	TBD	nS	
t_{ew}	Enable: WAIT after CSN ↓	20	80	90	nS	
t_{zd}	Disable: DQ after OEn ↑	TBD	TBD	TBD	nS	
t_{zp}	Disable: PDQ after OEn ↑	TBD	TBD	TBD	nS	
t_{zw}	Disable: WAIT after CSn ↑	TBD	TBD	TBD	nS	
t_{sa}	Setup: Address to CLK ↑	3			nS	
t_{sav}	Setup: ADVn ↓ to CLK ↑	3			nS	
t_{sbw}	Setup: BW#n to CLK ↑	TBD			nS	
t_{scr}	Setup: CRE to CLK ↑	3			nS	
t_{scs}	Setup: CSn ↓ to CLK ↑	TBD			nS	
t_{sd}	Setup: ADQ/DQ to CLK ↑	3			nS	
t_{sp}	Setup: PDQ to CLK ↑	3			nS	
t_{swe}	Setup: WEn to CLK ↑	3			nS	
t_{ha}	Hold: Address from CLK ↑	15			nS	
t_{hav}	Hold: ADVn ↑ from CLK ↑	15			nS	
t_{hbw}	Hold: BW#n from CLK ↑	15			nS	
t_{hcr}	Hold: CRE from CLK ↑	15			nS	
t_{hcs}	Hold: CSn ↑ from CLK ↑	TBD			nS	
t_{hd}	Hold: ADQ/DQ from CLK ↑	15			nS	
t_{hp}	Hold: PDQ from CLK ↑	15			nS	
t_{hwe}	Hold: WEn from CLK ↑	5			nS	

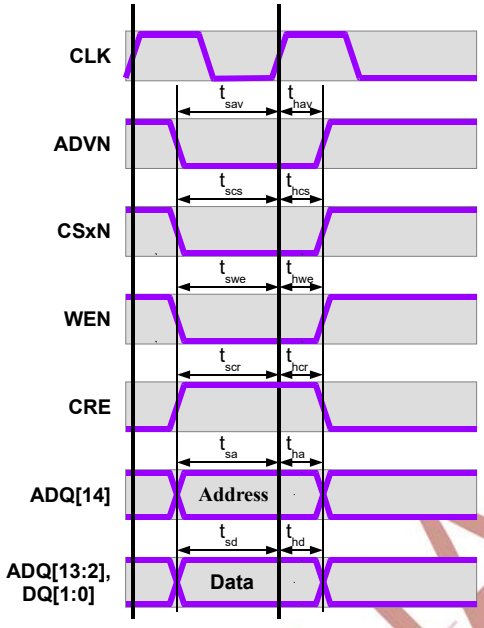


Figure 2: Configuration Write

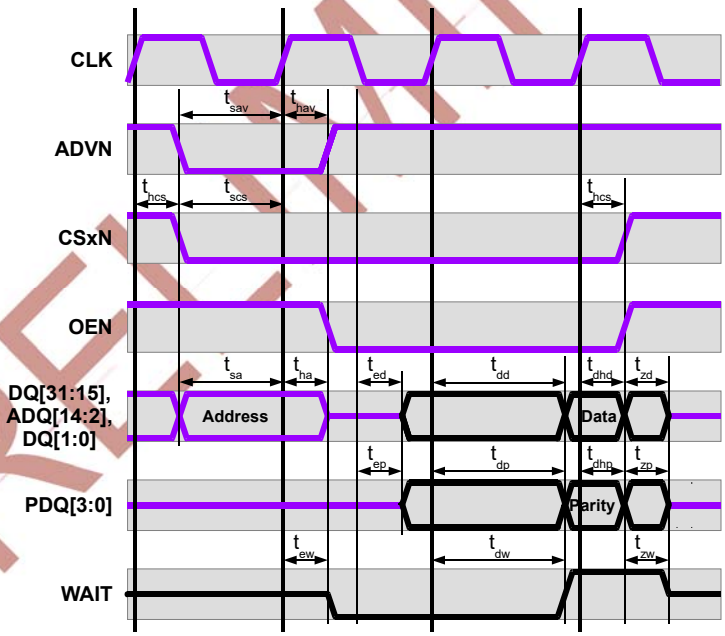


Figure 3: Read, Latency = 2 Cycles

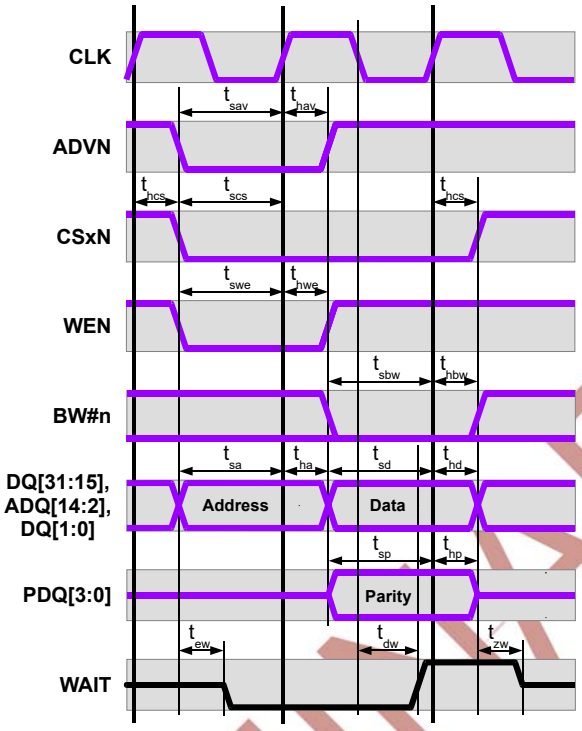


Figure 4: Write, Latency = 1 Cycle

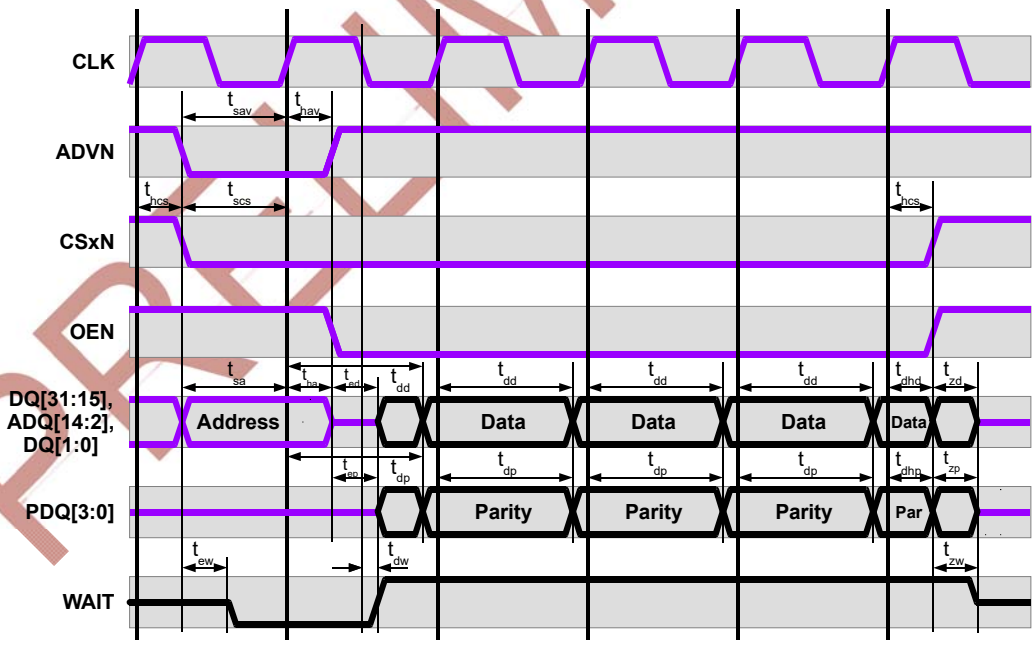


Figure 5: Read Burst, Latency = 1 Cycle

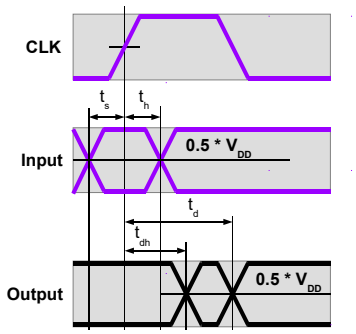


Figure 6: Delay Measurement

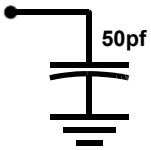
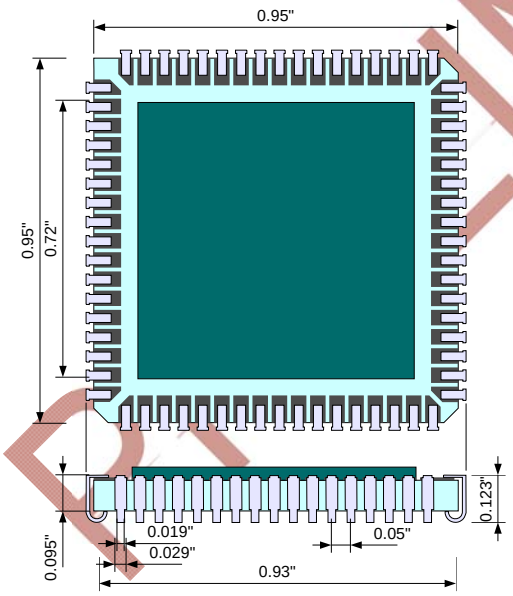


Figure 7: AC Measurement Load

PACKAGING

The RC2110836 is packaged in a 68 pin J-Lead Ceramic QFP.



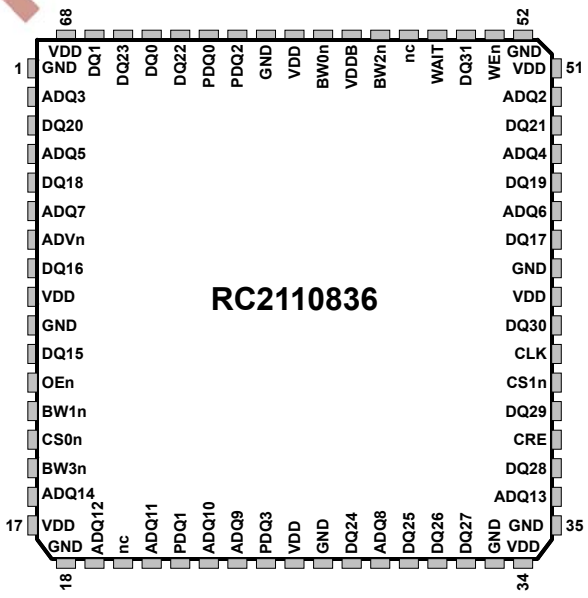


Table 7: Pin Out

Pin	Name	Dir	Function	Pin	Name	Dir	Function
1	GND	GND	Ground	35	GND	GND	Ground
2	ADQ3	I/O	Address/Data IO	36	ADQ13	I/O	Address/Data IO
3	DQ20	I/O	Data IO	37	DQ28	I/O	Data IO
4	ADQ5	I/O	Address/Data IO	38	CRE	In	Control Reg Enable
5	DQ18	I/O	Data IO	39	DQ29	I/O	Data IO
6	ADQ7	I/O	Address/Data IO	40	CS1n	In	Chip Enable
7	ADVn	In	Address Available	41	CLK	In	Clock
8	DQ16	I/O	Data IO	42	DQ30	I/O	Data IO
9	VDD	VDD	Power Supply	43	VDD	VDD	Power Supply
10	GND	GND	Ground	44	GND	GND	Ground
11	DQ15	I/O	Data IO	45	DQ17	I/O	Data IO
12	OEn	In	Output Enable	46	ADQ6	I/O	Address/Data IO
13	BW1n	In	Byte 1 Write Enable	47	DQ19	I/O	Data IO
14	CS0n	In	Chip Enable	48	ADQ4	I/O	Address/Data IO
15	BW3n	In	MSB Write Enable	49	DQ21	I/O	Data IO
16	ADQ14	I/O	Address/Data IO	50	ADQ2	I/O	Address/Data IO
17	VDD	VDD	Power Supply	51	VDD	VDD	Power Supply
18	GND	GND	Ground	52	GND	GND	Ground
19	ADQ12	I/O	Address/Data IO	53	WEn	In	Data Write Enable
20	nc	na	Not Connected	54	DQ31	I/O	Data IO
21	ADQ11	I/O	Address/Data IO	55	WAIT	T/S	Data Available
22	PDQ1	I/O	Byte 1 Parity	56	nc	na	Not Connected
23	ADQ10	I/O	Address/Data IO	57	BW2n	In	Byte 2 Write Enable
24	ADQ9	I/O	Address/Data IO	58	VDDB	VDDB	Battery Backup
25	PDQ3	I/O	MSB Parity	59	BW0n	In	LSB Write Enable
26	VDD	VDD	Power Supply	60	VDD	VDD	Power Supply
27	GND	GND	Ground	61	GND	GND	Ground
28	DQ24	I/O	Data IO	62	PDQ2	I/O	Byte 2 Parity
29	ADQ8	I/O	Address/Data IO	63	PDQ0	I/O	LSB Parity
30	DQ25	I/O	Data IO	64	DQ22	I/O	Data IO
31	DQ26	I/O	Data IO	65	DQ0	I/O	Data IO
32	DQ27	I/O	Data IO	66	DQ23	I/O	Data IO
33	GND	GND	Ground	67	DQ1	I/O	Data IO
34	VDD	VDD	Power Supply	68	VDD	VDD	Power Supply