FEATURES

- **-55°C to 300°C Temperature Range**
- 32K x 9 Random Access Memory
- 5-volt Operation
- 3.4-volt Battery Back Up
- Fully Static Design
- Parity Options
  - 8-Bit Data
  - 9-Bit Data
  - Even, Odd, or Sticky Parity
  - Parity Error
- Burst (4 word) or Single Operations
- RC10001 Compatible

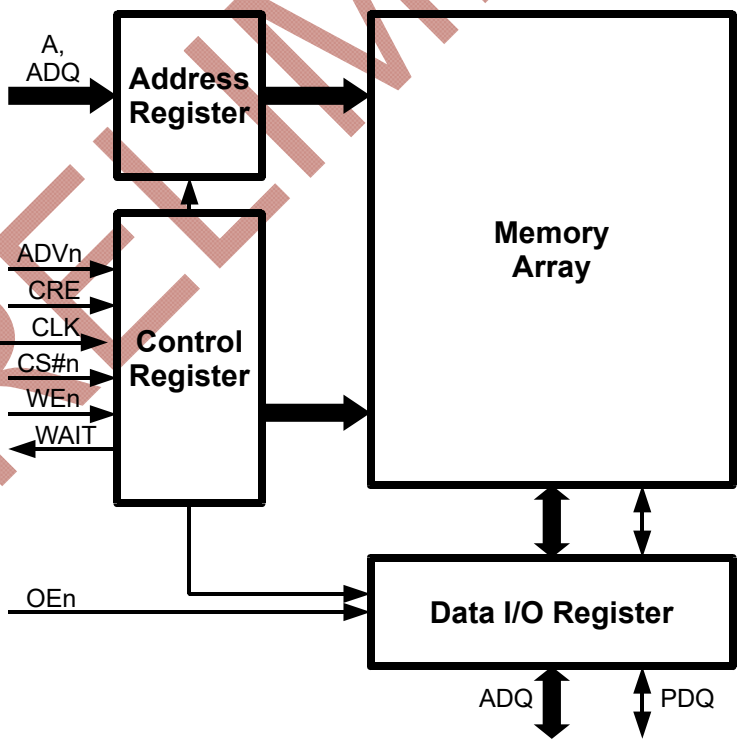

Figure 1: Block Diagram

DESCRIPTION

The RelChip® RC2113209 is a synchronous 32Kx9 RAM compatible with the RC10001 microcontroller. The memory is highly configurable, with options for parity, latency, and burst-mode. Fifteen bits of address (A [14:0]) are input during the address cycle.

Configuration

Product configuration is set by programming the configuration register (Table 1). The memory array is nine bits wide. Eight bits are data, and the ninth can be configured to be either parity or data. Parity bits are configured even, odd, or parity error. Latency, or the number of cycles from the address cycle to the data cycle, is programmable from one to eight cycles. A single address cycle can trigger a read or write of four bytes in the burst mode.

Configuration Register

The configuration consists of two registers of fourteen bits selected by A[14] (see Table 1). A special write of the configuration is used (Figure 2). The first register stores the latency and burst configuration, while the second stores the parity configuration.

Table 1: Configuration Register

A [14]	Bit	Symbol	Description	Default
0	13:11	Latency Count	Data Available in n+1 Clocks (See Table 2)	010
0	10:1	Reserved	Reserved	na
0	0	Burst Length	0=1, 1=4	1
1	13:3	Reserved	Reserved	na
1	2:0	Parity Selection	Parity Mode (See Table 3)	001

Latency

Latency can be programmed from one to eight cycles (see Table 1 and Table 2). Latency is the number of clock cycles from the address cycle to the data cycle (either read or write). Latency is configured with bits 13 through 11 of the first configuration register. The default value is three cycles.

Table 2: Latency Selections

Value (binary)	Latency (cycles)	Default
000	1	
001	2	
010	3	X
011	4	
100	5	
101	6	
110	7	
111	8	

Burst Mode

The RC2113209 can execute single or burst read or write operations for each address cycle. This mode is set in the configuration register (see Table 1). Burst operations begin at the address specified during the address cycle. Subsequent operations occur at the next address (modulo 4). If the operation is started with A[1:0] set to “00,” the part will use that address for the first operation, followed by “01,” “10,” and “11.” However, if the operations begin at A [1:0] equal to “10,” the sequence would then follow as “11,” “00,” and “01.” This operation will not modify A [2]. A burst operation is aborted by deselecting the part (CS0n or CS1n go high). An abort will not roll-back previous write operations. A burst will continue (with address wrapping) until the part is deselected.

Parity

The parity IO is configured through bits 2:0 in the configuration register (see Table 1). The Parity IO pin can be configured to floating, data, parity, or parity error flag.

The RC2113209 can be configured as a 8-bit part with parity, or as a 9-bit part without. As an 8-bit part, the parity IO pin (PDQ) is the parity pin for the data byte. For nine-bit operation, the parity IO pin is the ninth bit.

The RC2113209 will calculate the parity for each written byte, storing the value in the parity bit. The parity calculated is determined by the parity mode. For all parity modes, the bit is calculated and stored in memory.

When the part is read in even or odd parity modes, the parity value calculated during the write is reported on the PDQ pin. If the part is read in the parity error mode, the byte read has a new parity calculated. The PDQ pin is asserted when this new parity value is different than the stored one.

Table 3: Parity Selections

Value (binary)	Parity Bit	default
000	Z	
001	Data Bit 9	X
010	Even Parity	
011	Odd Parity	
1xx	Parity Error	

Status Register

There are, like the configuration register, two status registers. These are full 32-bit registers (see Table 4). The status includes all the configuration bits plus product identification fields.

Table 4: Status Register Contents

A [14]	A [1:0]	Bit	Register	Symbol	Description	Constant
0	11	7:0	31:24	Reserved	Reserved	0x00
0	10	7:0	23:16	Reserved	Reserved	0x00
0	01	7:6	15:14	Reserved	Reserved	00
0	01	5:3	13:11	Latency Cnt	Data Available in n+1 Clks (Table 2)	
0	01	2:0	10:8	Reserved	Reserved	101
0	00	7:1	7:1	Reserved	Reserved	0100000
0	00	0	0	Burst Length	0=1, 1=4	
1	11	7:0	31:24	Part Number	Integer	0x07
1	10	7:0	23:16	Part Number	Integer	0xD0
1	01	7:6	15:14	Reserved	Reserved	00
1	01	5:2	13:10	Configuration	Integer	0101
1	01	1:0	9:8	Rev Number	Integer 0-127	ROM
1	00	7:3	7:3	Rev Number	Integer 0-127	ROM
1	00	2:0	2:0	Parity Sel	Parity Mode (Table 3)	

Configuration Write

Configuration writes always occur in a single cycle (Figure 2). With the Configuration Register Enable (CRE) asserted high, a write operation is initiated. Address input 14 selects which of the two configuration registers is addressed. Address inputs 13 through 0 set the configuration bits.

Status Read

A status read is identical to a normal read except that the CRE pin is asserted high. The parity bit is always output as a low during a status read if enabled.

Read and Write with Latency

Adding latency to operations, whether burst mode or not, just adds cycles between the address cycle and the first operation cycle.

SPECIFICATIONS

Absolute Maximums (1)

Temperature..... -55 to 350ºC
Power Supply (V_{DD} referenced to ground) ..... -0.2 to 6.0 volts
Battery Voltage (V_{DDB} referenced to ground) ..... -0.2 to 6.0 volts
IO Voltage (referenced to ground) ..... -0.2 to 6.0 volts

Operating Conditions

Temperature (die temperature) ..... -55 to 300ºC
Power Supply (V_{DD} referenced to ground) ..... 4.5 to 5.5 volts
Battery Voltage (V_{DDB} referenced to ground) ..... 3.4 to (V_{DD}+0.1) volts
IO Voltage (referenced to ground) ..... -0.2 to (V_{DD}+0.2) volts

1. Exceeding the maximum specifications may cause permanent damage to the part

DC Characteristics

Table 5: DC Characteristics

Symbol	Description	Min	Typ	Max @225C	Max @300C	Unit	Note
V_{DD}	Digital Power Supply	4.5	5	5.5	5.5	V	
V_{DDB}	Battery Power Supply	3.4		V_{DD}+0.1	V_{DD}+0.1	V	1
I_{DD}	Active Current			2.5	3	mA/MHz	2
I_{DDS}	Standby Current (CSn=V_{DD})			1.5	2	mA/MHz	2,3
I_{DDB}	Battery Current (V_{DD}=0)			0.005	8	mA	4
V_{OH}	Digital Output High (I_{OH}=2mA)	0.9*V_{DD}				V	
V_{OL}	Digital Output Low (I_{OL}=2mA)			0.5		V	
V_{IH}	Digital Input High Voltage	0.8*V_{DD}				V	
V_{IL}	Digital Input Low Voltage			1.0		V	
I_I	Digital Input Current			10		uA	

Notes:

1. For systems not using battery backup, connect V_{DDB} to V_{DD}.
2. No Output Load
3. All bus signals toggling simulating other memories on the bus.
4. When not running on the battery, this DC current must be added to active and standby currents.

AC Characteristics

Table 6: AC Characteristics

Symbol	Description	Min	Max @225C	Max @300C	Unit	Note
F	Frequency		5	4	MHz	
t_{pw}	Pulse Width: CLK	80			nS	
t_{dd}	Delay: CLK ↑ to ADQ		120	130	nS	
t_{dp}	Delay: CLK ↑ to PDQ		120	130	nS	
t_{dw}	Delay: CLK to WAIT		75	80	nS	
t_{dhd}	Hold: ADQ after CLK ↑	20	100	110	nS	
t_{dhp}	Hold: PDQ after CLK ↑	20	100	110	nS	
t_{ed}	Enable: OEn ↓ to ADQ	TBD	TBD	TBD	nS	
t_{ep}	Enable: OEn ↓ to PDQ	TBD	TBD	TBD	nS	
t_{ew}	Enable: CSn ↓ to WAIT	20	80	90	nS	
t_{zd}	Disable: OEn ↑ ADQ	TBD	TBD	TBD	nS	
t_{zp}	Disable: OEn ↑ PDQ	TBD	TBD	TBD	nS	
t_{zw}	Disable: CSn ↑ to WAIT	TBD	TBD	TBD	nS	
t_{sa}	Setup: Address to CLK ↑	3			nS	
t_{sav}	Setup: ADVn ↓ to CLK ↑	3			nS	
t_{scr}	Setup: CRE to CLK ↑	3			nS	
t_{scs}	Setup: CSn ↓ to CLK ↑	TBD			nS	
t_{sd}	Setup: Data to CLK ↑	3			nS	
t_{swe}	Setup: WEn to CLK ↑	3			nS	
t_{ha}	Hold: Address CLK ↑	15			nS	
t_{hav}	Hold: ADVn ↑ from CLK ↑	15			nS	
t_{hcr}	Hold: CRE from CLK ↑	15			nS	
t_{hcs}	Hold: CSn ↑ from CLK ↑	TBD			nS	
t_{hd}	Hold: Data from CLK ↑	15			nS	
t_{hwe}	Hold: WEn from CLK ↑	5			nS	

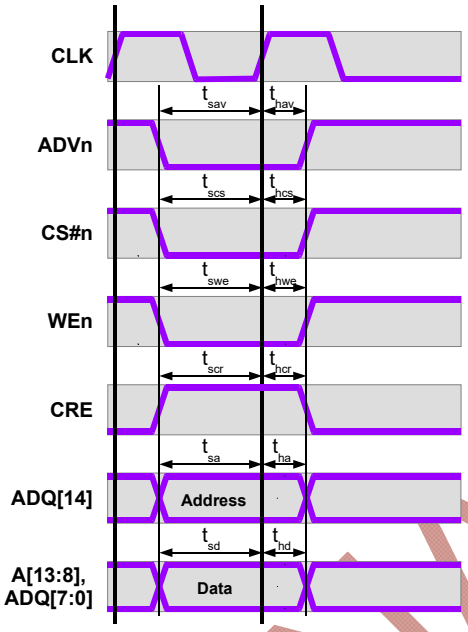

Figure 2: Write Configuration

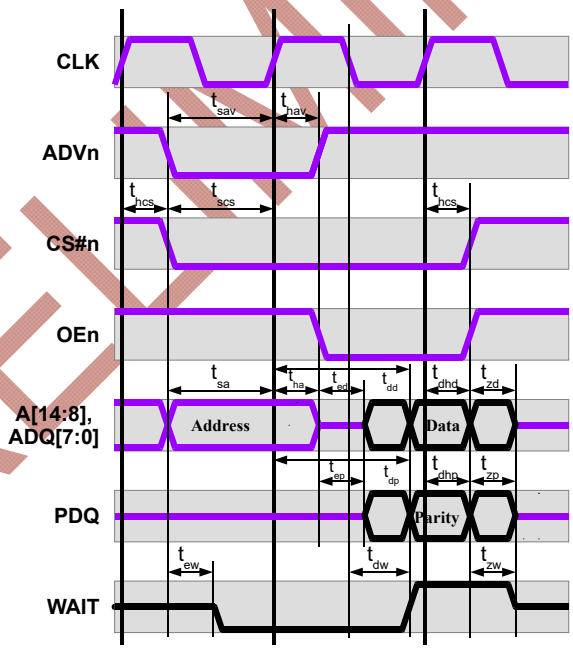

Figure 3: Read Timing, Latency = 1 Cycle

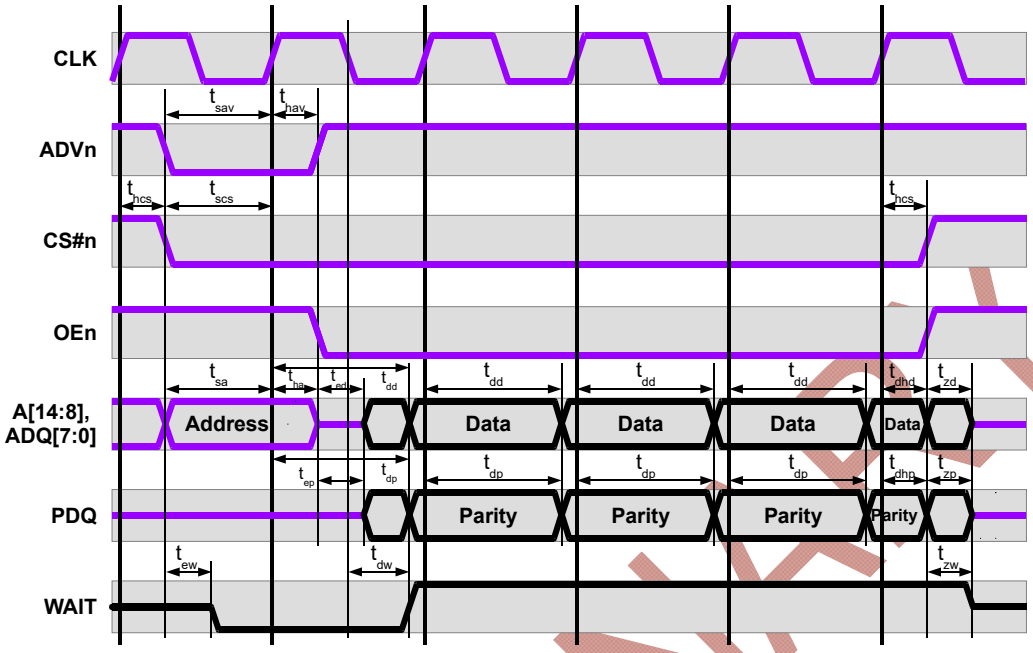

Figure 4: Read Burst Timing, Latency = 1 Cycle

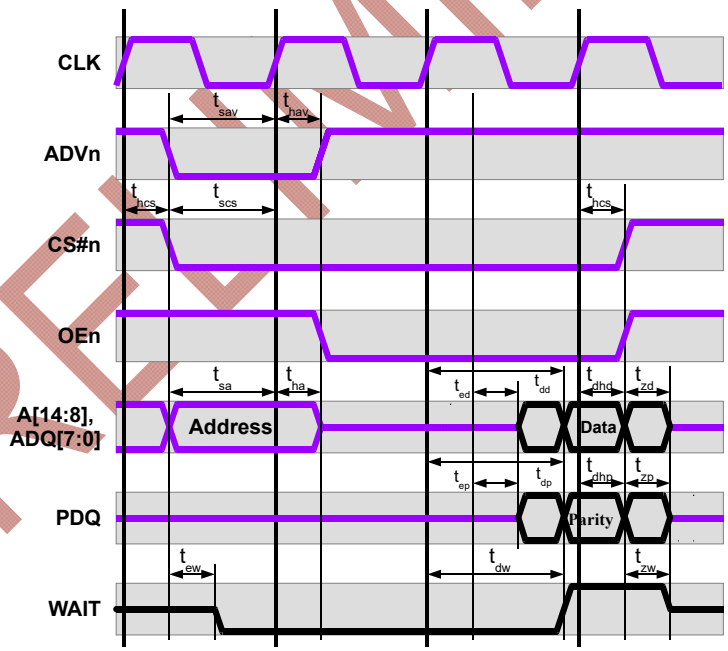

Figure 5: Read Timing, Latency = 2 Cycles

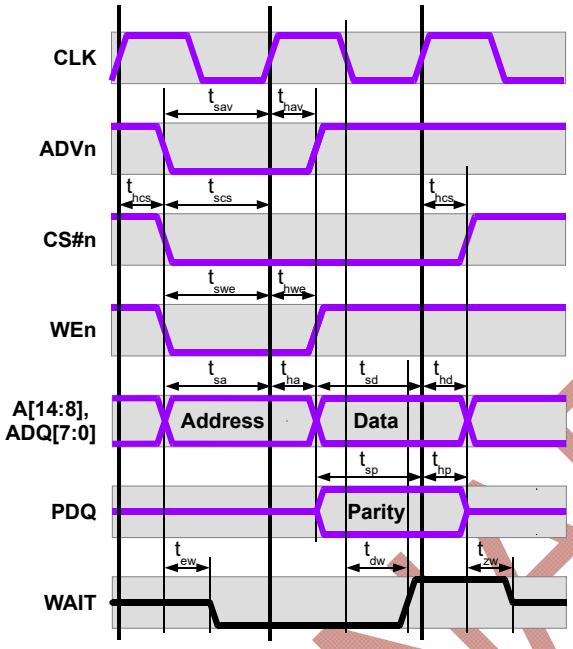

Figure 6: Write Timing, Latency = 1 Cycle

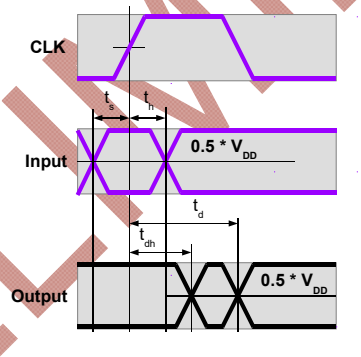

Figure 7: Delay Measurements

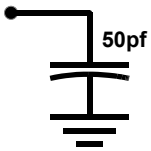

Figure 8: AC Load

PACKAGING

The RC2113209 is packaged in a 68 pin J-Lead QFP.

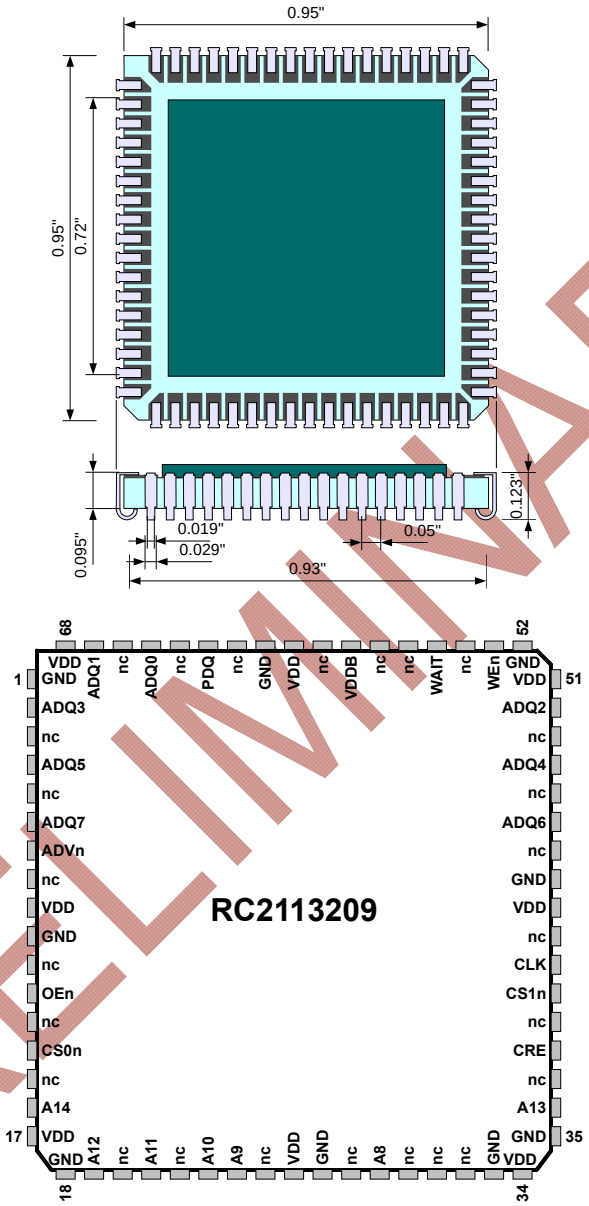

Table 7: Pin Out

Pin	Name	Dir	Function	Pin	Name	Dir	Function
1	GND	GND	Ground	35	GND	GND	Ground
2	ADQ3	I/O	Address/Data	36	A13	In	Address Input
3	nc	nc	No Connection	37	nc	nc	No Connection
4	ADQ5	I/O	Address/Data	38	CRE	In	Control Register En
5	nc	nc	No Connection	39	nc	nc	No Connection
6	ADQ7	I/O	Address/Data	40	CS1n	In	Chip Enable
7	ADVn	In	Address Valid	41	CLK	In	Clock
8	nc	nc	No Connection	42	nc	nc	No Connection
9	VDD	VDD	Power Supply	43	VDD	VDD	Power Supply
10	GND	GND	Ground	44	GND	GND	Ground
11	nc	nc	No Connection	45	nc	nc	No Connection
12	OEn	In	Output Enable	46	ADQ6	I/O	Address/Data
13	nc	nc	No Connection	47	nc	nc	No Connection
14	CS0n	In	Chip Enable	48	ADQ4	I/O	Address/Data
15	nc	nc	No Connection	49	nc	nc	No Connection
16	A14	In	Address Input	50	ADQ2	I/O	Address/Data
17	VDD	VDD	Power Supply	51	VDD	VDD	Power Supply
18	GND	GND	Ground	52	GND	GND	Ground
19	A12	In	Address Input	53	WEn	In	Write Enable
20	nc	nc	No Connection	54	nc	nc	No Connection
21	A11	In	Address Input	55	WAIT	T/S	Data Valid
22	nc	nc	No Connection	56	nc	nc	No Connection
23	A10	In	Address Input	57	nc	nc	No Connection
24	A9	In	Address Input	58	VDDB	VDDB	Battery Backup Supply
25	nc	nc	No Connection	59	nc	nc	No Connection
26	VDD	VDD	Power Supply	60	VDD	VDD	Power Supply
27	GND	GND	Ground	61	GND	GND	Ground
28	nc	nc	No Connection	62	nc	nc	No Connection
29	A8	In	Address Input	63	PDQ	I/O	Parity
30	nc	nc	No Connection	64	nc	nc	No Connection
31	nc	nc	No Connection	65	ADQ0	I/O	Address/Data
32	nc	na	No Connection	66	nc	na	No Connection
33	GND	GND	Ground	67	ADQ1	I/O	Address/Data
34	VDD	VDD	Power Supply	68	VDD	VDD	Power Supply