

FEATURES

- -55°C to 300°C Temperature Range
- 32K x 9 Random Access Memory
- 5-volt Operation
- 3.4-volt Battery Back Up
- Fully Static Design
- Parity Options
 - 8-Bit Data
 - 9-Bit Data
 - Even Parity
 - Odd Parity
 - Parity Error Bit

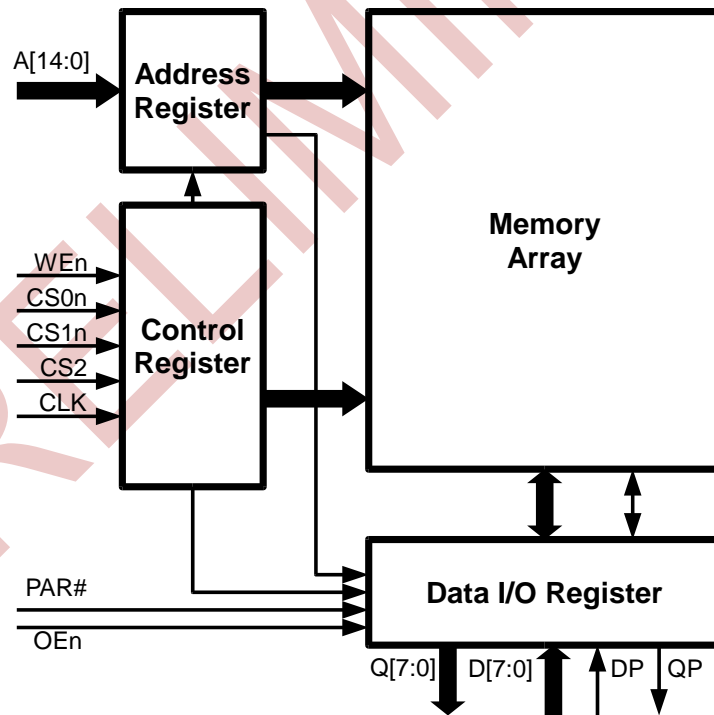


Figure 1: Block Diagram

DESCRIPTION

The RelChip® RC2133209 is a 32Kx9 RAM (288K bit). It supports either full 9-bit operation, or 8 bits with parity operation for high reliability applications. Many interfaces can be used since the part separates the data input, data output, and address pins. Data input and output lines may be tied together with external directional control using the OE signal.

Parity Configuration

The ninth data bit (on the DP/QP pin) is configured for data or parity by the PAR0 through PAR2 pins. These pins should all be tied high or low as required by the application. Table 1 shows the available configurations.

When a byte is written, parity bits are calculated and stored as the ninth data bit. When read, either that parity bit, or the comparison of the parity bit written and the parity of the read data is reported. Thus, parity can be checked by either the reading device, or by the RC2133209. A parity error, the comparison, is indicated by a high on the parity output.

Table 1: Parity Selections

PAR[2:0]	Parity Input	Parity Output
000	NA	Z
001	Data Bit 9	Data Bit 9
010	NA	Even Parity
011	NA	Odd Parity
1xx	NA	Parity Error

Read

Read occurs when WEn is not asserted on the rising edge of the CLK (see Figure 2).

Write

Write occurs when WEn is asserted on the rising edge of the CLK (see Figure 3).

SPECIFICATIONS

Absolute Maximums (1)

Temperature.....	-55 to 350°C
Power Supply (V_{DD} referenced to ground)	-0.2 to 6.0 volts
Battery Voltage (V_{DDB} referenced to ground)	-0.2 to 6.0 volts
IO Voltage (referenced to ground)	-0.2 to 6.0 volts

1. Exceeding the maximum specifications may cause permanent damage to the part

Operating Conditions

Temperature (die temperature).....	-55 to 300°C
Power Supply (V_{DD} referenced to ground)	4.5 to 5.5 volts
Battery Voltage (V_{DDB} referenced to ground)	3.4 to ($V_{DD}+0.1$) volts
IO Voltage (referenced to ground)	0.2 to ($V_{DD}+0.2$) volts

DC Characteristics

Table 2: DC Characteristics

Symbol	Description	Min	Typ	Max @225C	Max @300C	Unit	Note
T	Die Temperature	-55		225	300	°C	
V_{DD}	Digital Power Supply	4.5	5	5.5	5.5	V	
V_{DDB}	Battery Power Supply	3.4		$V_{DD}+0.1$	$V_{DD}+0.1$	V	1
I_{DD}	Active Current			2.5	3	mA/MHz	2
I_{DDS}	Standby Current (CS=deselect)			1.5	2	mA/MHz	2,3
I_{DDB}	Battery Current ($V_{DD}=0$)			0.005	8	mA	4
V_{OH}	Output High Voltage ($I_{OH}=4mA$)	$0.9 \cdot V_{DD}$				V	
V_{OL}	Output Low Voltage ($I_{OL}=4mA$)			0.5		V	
V_{IH}	Input High Voltage	$0.8 \cdot V_{DD}$				V	
V_{IL}	Input Low Voltage			1.0		V	
I_I	Input Current			10		uA	

Notes:

1. For systems not using battery backup, connect V_{DDB} to V_{DD} .
2. No Output Load
3. All bus signals toggling simulating other memories on the bus.
4. When not running on the battery, this DC current must be added to active and standby currents.

AC Characteristics

Table 3: AC Characteristics

Symbol	Description	Min	Max @225C	Max @300C	Unit	Note
F	Frequency		5	4	MHz	
t _{pw}	Pulse Width: CLK	80			nS	
t _{dq}	Delay: Q from CLK ↑		120	130	nS	
t _{eq}	Enable: OEn ↓ to Q	TBD	TBD	TBD	nS	
t _{zq}	Disable: OEn ↑ to Q	TBD	TBD	TBD	nS	
t _{sa}	Setup: Address to CLK ↑	3			nS	
t _{scs}	Setup: CS to CLK ↑	TBD			nS	
t _{sd}	Setup: Data to CLK ↑	3			nS	
t _{swe}	Setup: WEn to CLK ↑	3			nS	
t _{ha}	Hold: Address from CLK ↑	15			nS	
t _{hcs}	Hold: CS from CLK ↑	15			nS	
t _{hd}	Hold: Data from CLK ↑	15			nS	
t _{hwe}	Hold: WEn from CLK ↑	5			nS	

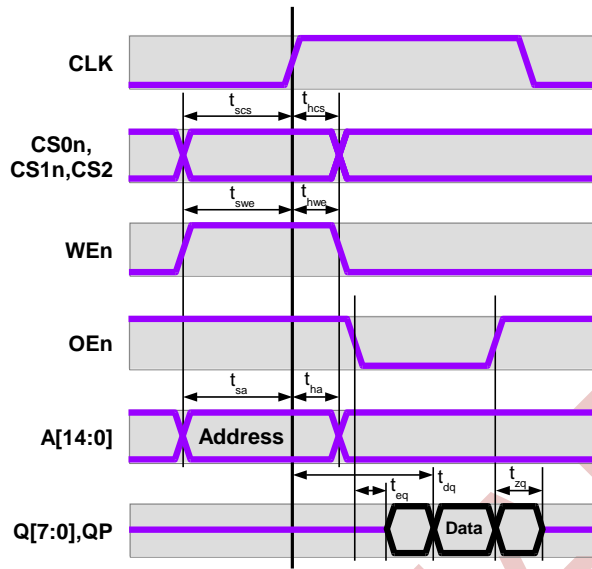


Figure 2: Read Timing



Figure 3: Write Timing

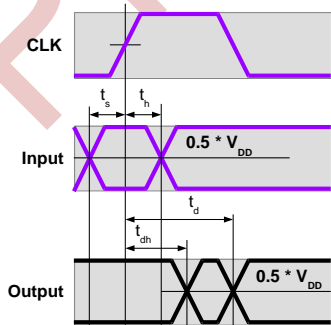


Figure 4: Delay Waveform

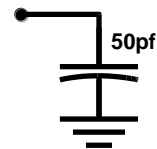


Figure 5: AC Load

PACKAGING

The RC2133209 is packaged in a 68 pin J-Lead QFP.

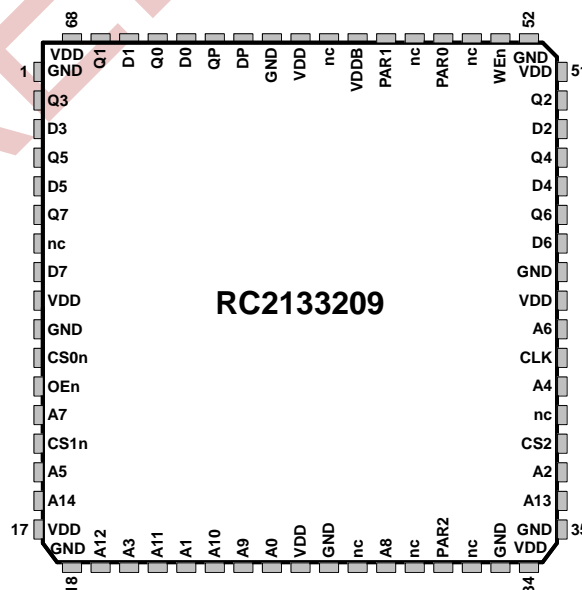
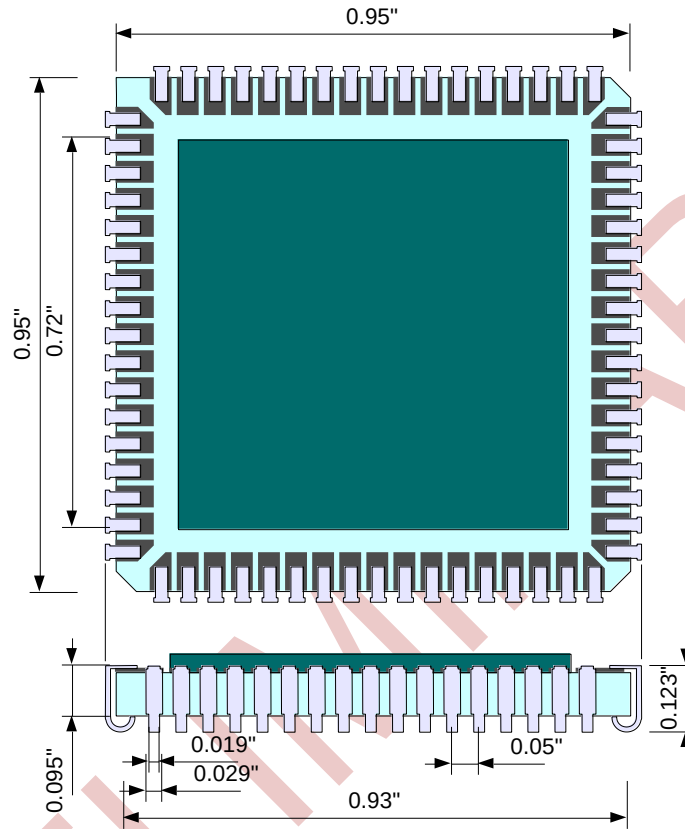


Table 4: Pin Out

Pin	Name	Dir	Function	Pin	Name	Dir	Function
1	GND	Ground	Ground	35	GND	Ground	Ground
2	Q3	TS	Data Output	36	A13	Input	Address Input
3	D3	Input	Data Input	37	A2	Input	Address Input
4	Q5	TS	Data Output	38	CS2	Input	Chip Enable
5	D5	Input	Data Input	39	nc	na	No Connection
6	Q7	TS	Data Output	40	A4	Input	Address Input
7	nc	na	No Connection	41	CLK	Input	Clock
8	D7	Input	Data Input	42	A6	Input	Address Input
9	VDD	Power	Power Supply	43	VDD	Power	Power Supply
10	GND	Ground	Ground	44	GND	Ground	Ground
11	CS0n	Input	Chip Enable (low active)	45	D6	Input	Data Input
12	OEn	Input	Output Enable (low active)	46	Q6	TS	Data Output
13	A7	Input	Address Input	47	D4	Input	Data Input
14	CS1n	Input	Chip Enable (low active)	48	Q4	TS	Data Output
15	A5	Input	Address Input	49	D2	Input	Data Input
16	A14	Input	Address Input	50	Q2	TS	Data Output
17	VDD	Power	Power Supply	51	VDD	Power	Power Supply
18	GND	Ground	Ground	52	GND	Ground	Ground
19	A12	Input	Address Input	53	WE _n	Input	Write Select (low active)
20	A3	Input	Address Input	54	nc	na	No Connection
21	A11	Input	Address Input	55	PAR0	Input	Parity Control Select
22	A1	Input	Address Input	56	nc	na	No Connection
23	A10	Input	Address Input	57	PAR1	Input	Parity Control Select
24	A9	Input	Address Input	58	VDD _B	Power	Battery Backup Supply
25	A0	Input	Address Input	59	nc	na	No Connection
26	VDD	Power	Power Supply	60	VDD	Power	Power Supply
27	GND	Ground	Ground	61	GND	Ground	Ground
28	nc	na	No Connection	62	DP	Input	Data 9 Input
29	A8	Input	Address Input	63	QP	TS	Parity Output
30	nc	na	No Connection	64	D0	Input	Data Input
31	PAR2	Input	Parity Mode	65	Q0	TS	Data Output
32	nc	na	No Connection	66	D1	Input	Data Input
33	GND	Ground	Ground	67	Q1	TS	Data Output
34	VDD	Power	Power Supply	68	VDD	Power	Power Supply

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