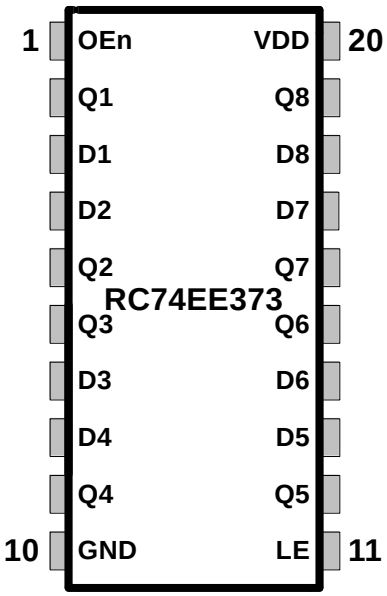
DESCRIPTION

The RelChip™ RC74EE373 is a transparent octal D-type latch designed for use in extreme environments. It is a functional and pin equivalent to the 74LS373.

The outputs can be put in high impedance state by the OEn pin. Latch transparency is controlled by LE.



FEATURES

- 5 volt Operation
- Fully Static Design
- Wide Operating Temperature Range

Table 1: Truth Table

D	OEn	LE	q1
X	1	X	Z
X	0	0	q0
0	0	1	0
1	0	1	1

X = don't care
Z = high impedance output

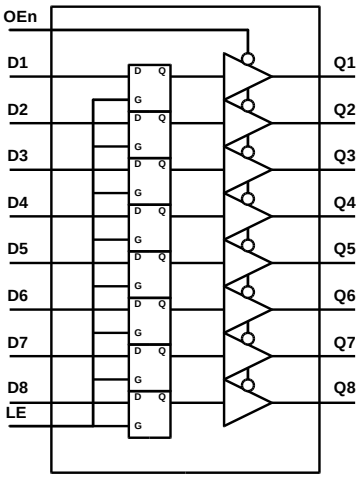


Figure 1: Block Diagram

SPECIFICATIONS

Absolute Maximums (1)

Temperature.....-55 to 350ºC
Power Supply (V_{DD} referenced to ground) ..... -0.3 to 6.0 volts
IO Voltage (referenced to ground) ..... -0.3 to 6.0 volts

Operating Conditions

Temperature (die temperature) ..... -55 to 300ºC
Power Supply (V_{DD} referenced to ground) ..... 4.5 to 5.5 volts
IO Voltage (referenced to ground) ..... -0.2 to (V_{DD}+0.2) volts

1. Exceeding the absolute maximum specifications may cause permanent damage to the part.

DC Characteristics

Table 2: DC Characteristics

Symbol	Description	Min	Typ	Max @225C	Max @300C	Unit	Note
T	Temperature (die)	-55	25	225	300	ºC	
V_{DD}	Power Supply	4.5	5	5.5	5.5	V	
I_{DD}	Active Current			2.0	2.2	mA/ MHz	1
I_{DDS}	Static Current (LE = 0)			50	50	uA	2
V_{OH}	Output High Voltage (I_{OH}=2mA)	0.85*V_{DD}				V	
V_{OL}	Output Low Voltage (I_{OL}=2mA)			0.5	0.5	V	
V_{IH}	Input High Voltage	0.8*V_{DD}				V	
V_{IL}	Input Low Voltage			1.0	1.0	V	
I_I	Input Current			10	10	uA	
I_{OZ}	Output Current (OEn = V_{DD})			20	20	uA	

Notes:

1. No Output Load
2. Leakage Driven Static Voltages (V_{DD} = 5.5v, Vin = V_{DD} and 0)

AC Characteristics

Table 3: AC Characteristics

Symbol	Description	Min	Max @225C	Max @300C	Unit	Note
t_{pw}	Pulse Width: LE	15			nS	
t_{ddq}	Delay: Data to Output		50	60	nS	
t_{dlq}	Delay: LE ↑ to Output		50	60	nS	
t_{dhq}	Hold: Output after LE ↑	0	10	10	nS	
t_{eq}	Enable: OEn ↓ to Output	20	40	50	nS	
t_{zq}	Disable: OEn ↑ to Output	20	40	50	nS	
t_{sd}	Setup: Data to LE ↓	7			nS	
t_{hd}	Hold: Data from LE ↓	1			nS	

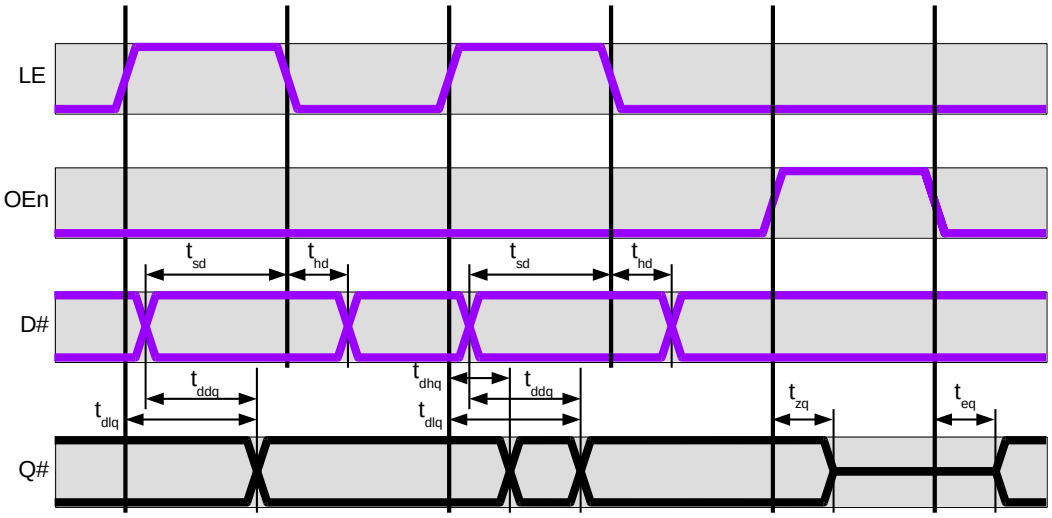


Figure 2: Timing Diagram

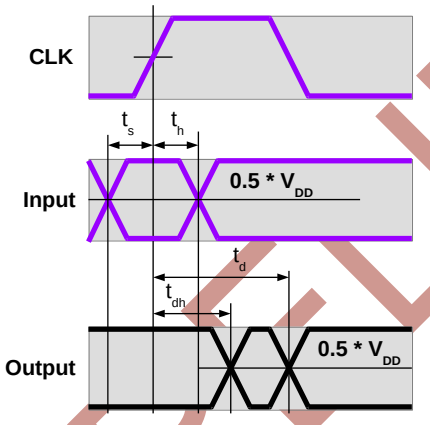


Figure 3: Delay Measurement

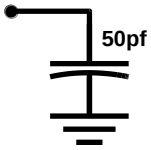


Figure 4: AC Measurement Load

PACKAGING

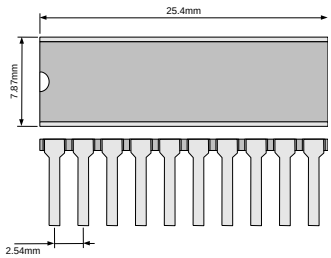


Figure 5: Ceramic DIP Package

Table 4: DIP Pin Out

Pin	Name	Dir	Function	Pin	Name	Dir	Function
1	OEn	Input	Output Enable	11	LE	Input	Latch Enable
2	Q1	Output	Data Output	12	Q5	Output	Data Output
3	D1	Input	Data Input	13	D5	Input	Data Input
4	D2	Input	Data Input	14	D6	Input	Data Input
5	Q2	Output	Data Output	15	Q6	Output	Data Output
6	Q3	Output	Data Output	16	Q7	Output	Data Output
7	D3	Input	Data Input	17	D7	Input	Data Input
8	D4	Input	Data Input	18	D8	Input	Data Input
9	Q4	Output	Data Output	19	Q8	Output	Data Output
10	GND	Ground	Ground	20	VDD	Power	Power Supply